OpenPA

The book of PA-RISC

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Bonn

Second Edition
Release 2.8
Bonn, May 2021

Other editions:
Second edition 2.7: July 2020
Second edition 2.6: January 2018
Second edition 2.5: January 2016
Second edition 2.4: July 2012
Second edition 2.3: July 2009
Second edition 2.2: January 2009
Second edition 2.1: October 2008
Second edition 2.0: May 2008
First edition 1.2: December 2007
First edition 1.1: November 2007
First edition 1.0: July 2006

Online OpenPA.nett is a registered serial publication with ISSN 1866-2757.

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Preface

This is the print edition of the **OpenPA.net** website from Spring 2021.

OpenPA is a resource for HP PA-RISC and Itanium computers with technical descriptions of workstations, servers, their hardware architecture and supported operating systems This project is independent of and does not represent The Hewlett Packard Company in any way.

This is the Second Edition 2.8.

Set with LaTeX.

Changes in Second Edition 2.8 since the last edition (2020):

- Many revisions and corrections (thanks!)
- Text and language in all chapters
- TeX backend update

All other changes are listed in chapter 5.1.

For the most current version of the OpenPA print edition please refer to
`http://www.openpa.net/print.html`.

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Chapter 1

Introduction

OpenPA is an information resource for HP PA-RISC based computers and technical architecture, a registered serial publication with ISSN 1866-2757.

PA-RISC is a RISC computer architecture designed by Hewlett-Packard in the 1980s and used in a range of HP 9000 and Visualize workstations and servers between the 1980s and 2000s. Some PA-RISC successors based on the HP/Intel Itanium architecture are also covered. This site is a non-commercial resource for information on these systems and technical details. First published in 1999, OpenPA is regularly updated with new or corrected content.

This book, now in its second edition, is the offspring of the online project OpenPA.net, a non-commercial information resource on PA-RISC computers. It is independent of The Hewlett Packard Company.

OpenPA.net was founded in December 1999 at a time when Google just started and Wikipedia did not exist yet. The idea was a central independent resource for information on PA-RISC Unix computers, widely available in the hobbyist market of the late 1990s and early 2000s. OpenPA development and contributions peaked in those early years between 1999-2002 with a lively community around PA-RISC and open source systems. Most PA-RISC and HP 9000 content on OpenPA was written and completed in the early 2000s, updates slowly declined from then on, as did PA-RISC support in open and commercial operating systems. OpenPA.net has been maintained in the two decades since to catch errors and add missing pieces here and there.

1999-2004

This site was started in 1999 when second-hand PA-RISC systems became affordable to collectors after being phased out for more modern 64-bit, Windows NT or Linux servers. Not a lot coherent PA-RISC information was available on the web when other popular Unix and RISC platforms were documented rather well. An 715/100 from a local newspaper ad started the interest and slowly led to a collection of PA-RISC documentation available on the web from the 1990s — much of it from the Mach and MkLinux projects. Compiled into a basic web site (with frames!), the information was soon published on the web, with hosting provided by Bill Bradford of SunHELP. The late Mickey appeared soon after, with lots of input from the OpenBSD/hppa operating system.

After two years, in 2001, the site was renamed to OpenPA.net and moved to its own Digital DECstation 5000 on 1Mb dialup. It has been written and maintained in vi (Nvi) in static HTML since, for more than two decades. The increasing support from HP for the PA-RISC Linux project made a lot official PA-RISC documentation available. Open source operating systems for PA-RISC made significant progress also, including version of OpenBSD and stock Linux. Most of the HP 9000/700 and

many of the "lettered" workstations were documented on OpenPA.net during that time, as were PA-RISC processors, chipsets and operating systems.

2005-2015

Updates became less frequent after 2005 with minor additions such as the PA-8800 and PA-8900 processors, PA-RISC architecture and operating systems. An OpenPA print edition was finally released with several hundred pages as PDF.

A spike of activity in 2008 resulted in lots of new content, with more PA-RISC systems such as the 64-bit workstations and rp Series servers, mainframes such as Convex SPP, V-Class and some early HP Itanium. Information on the fringes of PA-RISC was added also, including third-party PA-RISC processors and OEM systems from Japan and some very-early 1980s PA-RISC computers. Update frequency and additions stalled considerably after 2008 with mostly low-intensity maintenance.

2016-2021

Major housecleaning has been done several times beginning from 2016 on, checking links and content and rewriting much of the original language. Some new additions included the PA-RISC timeline and prices, a new print edition and restructuring several sections. Many pages were changed or updated, some ideas from previous years (decades) reversed and some severely outdated text updated or removed. There is still some old and original content scattered throughout, and many ideas to be implemented.

Much of the original HP documentation disappeared during that last decade, removing most of the links to original sources and references. Interest and support in open-source systems seemingly dwindled also. There is still a story to be written around PA-RISC, HP 9000 and the opening up of the 1990s and 2000s. We'll see.

People

Paul Weissmann is the maintainer and author of OpenPA. Many people helped OpenPA with contributions and support over the years. Thanks go to:

- Bill Bradford, for hosting this site in its early days
- Dave Fotland, for the PA-7200 and HP 9000/840 information
- Dennis Grevenstein, for information and documentation on the early HP 9000/800s
- Frank McConnell, for the HP 9000/500 and FOCUS information
- GÃűtz Hoffart, for the CSS/HTML help and inspiration
- Grant Grundler, for his support with HPPA and PA-RISC Linux over the years
- Michael Piotrowski, for corrections and HP-UX background information
- Michael Shalayeff âIJİ, for providing PA-RISC and general wisdom
- Mike Hibler, for information on HPBSD content and Utah University operating systems
- Miod Vallat, for various PA-RISC explanations
- Ruby Lee, for the PA-RISC Stirling information

- Thibaut Varene, for PA-RISC Linux help and the development section
- Ti Kan, for the technical explanations on the Stratus architecture
- Various contributors and readers that sent in corrections, clarifications and questions

Copyright

Sources

The information on OpenPA.net is based mostly on primary HP sources such as HP and PA-RISC technical reference manuals, handbooks and architecture documents from the 1990s. This was extended and correlated during the 2000s with secondary sources like magazine articles, news releases and journals like the HP Journal. Since many original sources and documents disappeared during the 2010s, much of the newer content of the last years is based more on secondary sources and industry articles.

PA-RISC CPU, chipset and architecture: Mostly made use of primary sources from HP, like the great HP "External Reference Specifications" (ERSs), and technical publications from HP CPU and chip design labs, that often were made available during the 2000s for HP-supported open source projects. Secondary sources in the form of articles or academic papers were used as well.

Computer systems: Information on the HP 9000 and PA-RISC computers is based on primary sources from HP and vendors in the form of system user guides, technical handbooks and architecture white papers. Also included in the research and collection were marketing brochures, news articles and industry reporting.

Operating systems: Depending on the system, either based on official vendor user and admin documentation as well as academic papers, talks, whitepapers and such. The heydays of open source, Mach, Linux and BSD research systems from the 1990s resulted in much information on public websites. Much of the operating system development on PA-RISC centered on the 1990s, information is getting sparse.

"The Internet never forgets:" A process that had started in the mid-2000s accelerated in the 2010s — many sources and information on the web from the 1980s and 1990s disappeared. Journals closed or lost their archives, websites vanished, companies merged and removed old documentation and websites in the process, and memory faded after all those decades. This pertained to most original HP documentation on HP 9000 and PA-RISC, contemporary news articles from the 1990s, news releases, price lists and so on.

It got quite difficult since then to write and update articles based on ever fluctuating sources. This might just be the transitional nature of the Internet, but it was surprising to see so much go after doing this for two decades.

Chapter 2

PA-RISC Design

2.1 Overview

The computers covered by this site are based on HP PA-RISC architecture and processors from the 1980s to 2000s. Most of the chipsets and system designs used were custom HP for its PA-RISC servers and workstations.

The following PA-RISC components are covered with individual articles:

- PA-RISC Processors: HP developed more than a dozen 32-bit and 64-bit PA-RISC processors, from the early PA 1.0 to the PA-7000 and PA-8000 families.
- PA-RISC Architecture: Details of PA-RISC architecture and processors.
- Chipsets: HP PA-RISC computers used proprietary HP chipsets and system designs, usually specific to a group of processors and computers.
- Buses: Many custom HP buses were used in PA-RISC for processors, memory and I/O devices, like GSC, VSC and HP-PB but also industry standard such as EISA and PCI.
- SCSI Controllers: Storage used industry-standard SCSI buses and third-party SCSI controllers.
- Graphics adapters: HP sold PA-RISC with its own range of CRX and Visualize graphics adapters.

2.1.1 Hardware phases

Hardware components and system designs used in PA-RISC computers by HP can be divided roughly in four phases in the PA-RISC history from the 1980s to the mid-2000s.

Table 2.1: PA-RISC hardware period table

Period	Processors	Design	Chips
I	Infancy: Early Architecture		
	TS-1, NS-1, NS-2, PCX	Early	SIU/SPI, CTB
II	Growth: 32-bit 1990s		
	PA-7000, PA-7100	ASP/Viper	Viper. ASP
III	Maturity: The heydays		
	PA-7100LC, PA-7300LC	LASI	MIOC, LASI, Wax, Dino
	PA-7200, PA-8000, PA-8200	U2/UTurn	MMC/SMC, U2, UTurn,LASI, Wax, Dino, Cujo
	PA-8500, PA-8600, PA-8700	Astro	Astro, Elroy
		Stretch	DEW, Prelude, IKE, Elroy
IV	Decline: 64-bit to Itanium		
	PA-8700, PA-8800PA-8900	Cell	CC, XBC, SBA, Elroy
	PA-8800PA-8900, Itanium 2	zx1	Pluto, Mercury

Infancy (I)

Early Precision Architecture of the late 80s. First versions of PA-RISC were released in the late 1980s as Precision Architecture with early implementations of processors and chipsets for the early HP 9000 800 series of computers. A few systems were released, but details on their exact architecture remain fuzzy. These designs were quickly superseded by new designs for both servers and workstations in the 1990s.

Systems sold in that period used PA-RISC processors such as TS-1, NS-1, NS-2 and PCX and were based

on custom HP system designs. Chipsets used were the SIU/SPI main bus interfaces that connected the processors to the SMB bus that links it to memory, I/O and devices. In most cases the system processing and I/O units are made up of a large number of individual chips or boards forming the central chipset with the CIO and HP-PB I/O buses.

Growth (II)

32-bit PA-RISC in the early 1990s. PA-RISC workstations and servers became popular with PA version 1.1 processors and new chipsets and system designs built on it.

Major innovations and developments took place from the late 1980s to the early 1990s to produce the PA-RISC 1.1 architecture and popular Unix systems based on it from the early 1990s on. They did not have much in common with the early PA-RISC 1.0 systems.

Along with the architecture, PA-RISC hardware designs matured throughout the early 1990s, with popular 32-bit PA-7000 and PA-7100 systems using the ASP chipset and Viper memory controller. They utilize the VSC CPU/memory, GSC system main and SGC and EISA expansion buses, with servers using HP-PB I/O buses, all provided by separate I/O adapters/bus bridges.

Maturity (III)

The PA-RISC heydays in the 1990s. Many innovations and improvements took place in the heydays of PA-RISC in the 1990s, with 32-bit low-cost LC processors, a shift to 64-bit PA-RISC 2.0 and quite advanced designs and I/O components.

From the mid-1990s on, the integrated, "low-cost" PA-7100LC and PA-7300LC systems use the highly integrated LASI chipset, which combines most functions and I/O on a single chip, and an on-CPU MIOC memory controller. These system use GSC or GSC+ as main bus and a variety of expansion buses via bus adapters, ranging from HSC/GSC, EISA to PCI and VME. EISA is provided by Wax, PCI by Dino.

PA-7200 and 64-bit PA-8000 and some PA-8200 systems use the U2/Uturn I/O adapters, which attach two GSC/HSC buses to the main Runway bus, and MMC/SMC memory controllers. I/O is realized on the GSC bus with the LASI chipset and Wax and Dino I/O adapters.

PA-RISC computers from the turn of the century used 64-bit PA-8500, PA8600 and PA-8700 designs with a "rope" -based architecture with Astro as main system controller and separate Runway+/Runway DDR buses with I/O devices controlled by Elroy PCI bridges.

Midrange servers from that time are based on the same processors (PA-8500 to 8700) but use the sophisticated Stretch chipset, a rather complicated setup with central system controller and links to separate processor and I/O controllers and PCI bridges. Main system bus is the Itanium bus, with converters for the processors' Runway+/Runway DDR buses.

Decline (IV)

64-bit to Itanium in the 2000s. HP transitioned to a "post-RISC" phase in the 2000s, releasing the last PA-RISC 2.0 processors and introducing Itanium to its server and workstation lineup. System designs converged between PA-RISC and Itanium.

PA-RISC moved towards a server-only role in the early 2000s, with a variety of servers in the rp-range and the similar Superdome mainframe. The Superdome "mainframes" and similar servers are based

on PA-8700 and PA-8800/PA-8900 processors and use the Cell chipset, similar to the Stretch, but more scalable. Systems are made up of "cells" , with their own central system/memory controller, I/O controller and PCI bridges.

The last PA-RISC systems before the mainstream advent of the Itanium VLIW architecture in the mid-2000s use PA-8800/PA-8900 processors, followed by several generationis of Itanium systems. Both use the HP zx1 chipset, conceptually similar to Astro systems but with higher datarates and options, based on Itanium 2/McKinley buses.

2.2 Overview

The PA-RISC platform is based on RISC processors from HP and was used in HP computers from the 1980s to the mid-2000s. Three major revisions of the PA-RISC architecture were developed:

1. **PA-RISC 1.0** 32-bit, implemented in several early processors and used in the very first PA-RISC servers in the 1980s, without MMU: NS-1, NS-2 and PCX, plus the TTL TS-1 and possible CS-1.
2. **PA-RISC 1.1** 32-bit, used in HP 9000 servers and workstations from the late-1980s and 1990s: the first PA-7000 and PA-7100 and the later integrated "low-cost" PA-7100LC and PA-7300LC.
3. **PA-RISC 2.0** 64-bit, extended PA-RISC with a redesign of most parts of the architecture, used in the late-1990s to 2000s in many PA-RISC computers: PA-8000 and PA-8200 (very similar) and the modified iterations PA-8500, PA-8600 and PA-8700 with large on-chip caches. PA-8800 and PA-8900 are dual-core chips, with the last PA-9000 never implemented.

The following PA-RISC processors have been developed and used by HP throughout the years.

Table 2.2: HP PA-RISC processors overview

CPU	ISA	Release	Clock max	Cache max	Bus	Super scalar	SMP	Units
TS-1	PA 1.0 32-bit	1986	8MHz	128KB	Custom	1-way		1 Integer 1 external FPU
NS-1	PA 1.0 32-bit	1987	30MHz	128KB	SMB	1-way		1 Integer 1 external FPU
NS-2	PA 1.0 32-bit	1989	27.5MHz	1MB	SMB	1-way	Yes	1 Integer 1 external FPU
PCX	PA 1.0 32-bit	1990	50MHz	1MB	SMB	1-way	Yes	1 Integer 1 external FPU
PA-7000	PA 1.1a 32-bit	1991	66MHz	512KB	PBus/VSC	1-way		1 Integer 1 external FPU
PA-7100 PA-7150	PA 1.1b 32-bit	1992	125MHz	3MB	PBus/VSC	2-way	Yes	1 Integer 1 Floating Point
PA-7100LC	PA 1.1c 32-bit	1994	100MHz	1KB 2MB L2	GSC	2-way		2 Integer 1 Floating Point *MAX-1*
PA-7200	PA 1.1d 32-bit	1995	140MHz	2KB 3MB L2	Runway	2-way	Yes	2 Integer 1 Floating Point
PA-7300LC	PA 1.1e 32-bit	1996	180MHz	128KB 8MB L2	GSC	2-way		2 Integer 1 Floating Point *MAX-1*
PA-8000	PA 2.0 64-bit	1996	230MHz	2MB	Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store *MAX-2*
PA-8200	PA 2.0 64-bit	1997	300MHz	4MB	Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store *MAX-2*
PA-8500	PA 2.0 64-bit	1998	440MHz	1.5MB	Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store *MAX-2*

PA-8600	PA 2.0 64-bit	2000	550MHz	1.5MB	Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store *MAX-2*
PA-8700	PA 2.0 64-bit	2001	875MHz	2.25MB	Runway	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store *MAX-2*
PA-8800 dual-core	PA 2.0 64-bit	2004	1GHz	2×1.5MB 32MB L2	Itanium 2	2×4-way	Yes	2 cores, each: 4 Integer 4 Floating Point 2 Load/Store *MAX-2*
PA-8900 dual-core	PA 2.0 64-bit	2005	1.1GHz	2×1.5MB 64MB L2	Itanium 2	2×4-way	Yes	2 cores, each: 4 Integer 4 Floating Point 2 Load/Store *MAX-2*

2.2.1 Early PA-RISC processors

The first PA-RISC processors were designed and used in mid to late-1980s in early HP 9000/800 servers and HP 3000 MPE/iX systems. The exact naming scheme is not totally clear as some sources refers to these processors as **TS-1**, **NS-1** and **NS-2** while others call apparently the same processors **PN-5**, **PN-7** and **PN-10**. These early CPUs still mostly were multi-chip processors with separate chips and components forming the central processing unit, contrary to the mostly single-chip post-PA-7000 implementations. The chips were based on TTL manufacturing, then NMOS-III and finally CMOS26B. An interesting aspect of these CPUs is their huge TLB — from 2048 up to 16384 entries while their successors and competitors had sizes typically in the low to mid hundreds.

TS-1 processor

The TS-1 was the first PA-RISC production processor, introduced in 1986. It integrated version 1.0 of PA-RISC on six 8.4×11.3″ boards of TTL and was used in HP 9000 840 servers, the first PA-RISC computers.

- PA-RISC version 1.0 32-bit, three-stage pipeline
- The CPU consists of six separate boards:
    1. I-unit Instruction Unit
    2. Register File Board, contains general and control registers
    3. E-unit Execution Unit
    4. TLB translation lookaside buffer with 4096 entries for 2 KB pages
    5. Cache controller with split instruction and data caches of 64 KB each
    6. FPC floating-point coprocessor, handles FP operations parallel to the CPU/ALU (ADD/MUL/DIV chip was taken over from HP 9000/550 FOCUS)
- TLB off-chip, direct-mapped, 4096 entries
- L1 cache off-chip 128 KB I/D direct-mapped/one-way associative
- Physical address space of 27-bit, 128 MB main memory could be addressed
- Clock speed 8 MHz
- Six or five printed circuit boards, implemented in FAST TTL and 25ns/35ns SRAMs/PALs, with each about 150 ICs

NS-1 processor

The first implementation of PA-RISC in a NMOS fabrication process, NS-1, followed in 1987 shortly after the original TTL-based TS-1. The NS-1 processor is integrated on a single circuit board (two on 825 servers) with the CPU as single NMOS-III chip supplemented by external support chips. It was used in: HP 9000 825, 835, 850 servers.

- PA-RISC version 1.0 32-bit, three-stage pipeline
- Single CPU with eight support VLSI chips
    1. SIU system interface unit attaches the CPU to the SMB main bus

2. CCU cache controller units CCU0 and CCU1 attach to external cache
3. TCU TLB controller unit attaches to the external TLB
4. MIU math interface unit with three third-party FP chips ADD, MUL and DIV

- ◈ TLB off-chip with 2048 to 4096 entries
- ◈ L1 cache 16 KB to 128 KB, unified and off-chip
- ◈ Physical address space of 29-bit, 512 MB main memory could be addressed
- ◈ CPU attaches via System Main Bus SMB to memory and I/O controllers, 64-bit bus
- ◈ Clock speed 25-30 MHz
- ◈ One circuit board, two boards on HP 9000/825, 144,000 FETs, implemented in NMOS-III in a 272-pin ceramic PGA package

NS-2 processor

The final NMOS PA-RISC processor was the NS-2, a tweaked follow-on to the NS-1 introduced in 1989-90 with from three to five stages increased pipeline, new TLB and cache controllers and significantly larger caches and TLB. The NS-2 is implemented on one circuit board with the CPU as a single NMOS-III and seven other VLSI chips. The bus structure connecting these chips was updated and simplified, with the CPU having private connections to the cache and TLB controllers, for which the NS-1 CPU had to use the shared cache bus.

The NS-2 was used in the HP 9000/822 and 832 and the 845, 855, 860 servers.

- ◈ PA-RISC version 1.0 32-bit, five-stage pipeline
- ◈ CPU is a single chip with seven VLSI support chips
  1. SIU system interface unit, attaches the CPU to the SMB main bus
  2. CCU cache controller units ICCU and DCCU, attach to external cache chips
  3. TCU TLB controller unit, attaches to external TLB chips
  4. FPC floating point controller and two third-party FP chips ADD, MULTI
- ◈ TLB off-chip, 16384 entries
- ◈ L1 cache up to 1024 KB, split into I/D, off-chip
- ◈ Physical address space of 29-bit, 512 MB main memory could be addressed
- ◈ CPU attaches via System Main Bus SMB to memory and I/O controllers, synchronous, pipelined 64-bit bus
- ◈ Clock speed 27.5 or 30 MHz, power dissipation of 26W
- ◈ One circuit board, CPU implemented in NMOS-III, 183,000 FETs, 1.5µNMOS-III, die size 14.0×14.0 mm^2 die, packaged in 408-pin PGA

PCX (CMOS26B) processor

The last PA-RISC 1.0 design was the PCX, introduced 1990 and the first PA-RISC processor fabricated in a CMOS process. It implemented the NS-1/NS-2 design and several of the processor functions previously supplied on external VLSI chips onto a single CPU chip. The PCX was also supplemented by external support chips, including three cache multiplexers, the SPI main bus to processor interface, an floating point coprocessor and two FP chips for MUL/DIV and ADD/SUB. The successor to the PCX was the PA-RISC 1.1 PCX-S or PA-7000 processor, which integrated most processor logic minus the FPU onto a single die/chip

PCX was used in the HP 9000/808, 815 and HP 9000/842, 852, 865, 870 servers.

- PA-RISC version 1.0 32-bit
- First multi-processor-capable PA-RISC CPU, up to four-way SMP
- Seven external supported chips
- External FPU (apparently ECL logic)
- TLB on-chip with 8192 entries
- L1 cache off-chip 1024 KB, split into I/D apparently asymmetrical 1:2
- Physical address space of 29-bit, 512 MB main memory could be addressed
- CPU attaches via System Main Bus SMB to memory and I/O controllers, 64-bit bus
- Clock speed 50 MHz
- One circuit board, 196,000 FETs, 1.0µ(micron), implemented in three-level CMOS26B
- CPU is a single chip, needs seven other VLSI support chips for memory/bus interfaces and I/O

Some sources mention a "CS-1" processor — CS would point to a CMOS design but the performance figures and diagrams do not really match up with the **CMOS26B/PCX** *described here.*

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2.2.2 PA-7000 (PCX-S) processor

Overview

The PA-7000 was a 32-bit PA-RISC processor, version 1.1 architecture with a MMU, introduced in 1991. It was first used in the HP 9000 700 series workstations and later in some of the HP 9000 800 Nova servers. The PA-7000 was a multi-chip implementation with an external FPU.

Details

- PA-RISC version 1.1a, 32-bit architecture
- Two functional units: 1 integer ALUs, 1 external FPU
- Five-stage pipeline
- TLB: 192 in I/D; BTLB: 8 in I/D
- Cache L1 256 KB I and 256 KB D off-chip
- Memory and I/O controllers are external
- PBus processor bus, 32-bit, from processor to the Memory and I/O Controller MIOC
- Up to to 66 MHz closck speed with 5.0 V core voltage
- 14.2×14.2 mm^2 die, 577,000 FETs, 1.0µ, 2-layer CMOS26B in 408-pin CPGA
- External FPU fabbed in 13.0×13.0 mm^2 die, 640,000 FETs, 0.8µ, TI EPIC-2 in 207-pin CPGA

Used in

- HP 9000 705, 710, 720, 730, 750 workstations
- HP 9000 F10, F20, F30, G30, G40, H20, H30, H40, I30, I40 servers
- HP 9000 890 mainframe
- Mitsubishi ME/R7200, ME/S7200, ME/R7300, ME/S7300, ME/R7500, ME/S7500 workstations

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2.2.3 PA-7100/PA-7150 (PCX-T) processor

Overview

The PA-7100 was the first PA-RISC processor to integrate the Integer ALU and FPU on a single die. It was introduced in 1992, with the enhanced PA-7150 in 1994. The design of the integer units is close to the PA-7000 but modified to scale to higher clock speeds. The previously external FPU was a new design and moved on chip, taking about one third of the transistor count. The link between the PA-7100 and its instruction cache was doubled in width compared to the PA-7000. The PA-7100 is a superscalar processor that is able to issue two separate instructions at a time. It was used in a large range of 1990s HP 9000 workstations and servers.

Multi-processor systems could be designed with two astrategies: either two PA-7100s attach to a shared PBus and one Viper Memory and I/O Controller, or each PA-7100 is attached to its own MIOC, which in turn is attached to a shared memory and I/O bus with the other PA-7100/MIOCs.

The PA-7150 is a PA-7100 with tweaks to the core and cache subsystem to allow clock frequencies up to 125 MHz.

Details

- PA-RISC version 1.1b, 32-bit architecture, multi-processor capable, 2-way superscalar
- Two functional units: 1 integer ALUs, 1 FPU
- Five-stage pipeline
- 3-instruction queue
- TLB: 120-entry fully associative; BTLB: 16-entry
- Cache L1 up to 1 MB I and 2 MB D in asynchronous standard SRAMs
- CPU, FPU, MMU and cache controller on one chip, memory and I/O controller Viper MIOC, off-chip
- PBus processor bus, 32-bit, from processor to the Memory and I/O Controller MIOC
- Up to to 100 MHz, 125 MHz on the PA-7150, clock speed with 5.0 V core voltage
- 14.0×14.0 mm^2 die, 850,000 FETs, 0.8µ, 3-layer metal CMOS26B in a 504-pin ceramic PGA, 30W power at 100 MHz

Used in

- HP 9000 *715*, *725*, *735*, *755*, *742*i, *745*i, *747*i workstations
- HP 9000 G50, G60, G70, H50, H60, H70, I50, I60, I70 servers
- HP 9000 T500, T520 mainframes
- Convex SPP1000/CD, SPP1000/XA mainframes
- Hitachi 3050RX 220, 230, 310S, 320, 330, 430, 440, 9000V V735/125, VT500 workstations
- Stratus Continuum 610S, 610, 615S, 615, 620, 625, 1220, 1225, 1245 mainframes

References

1. A 200 MFLOP HP PA-RISC Processor (.pdf) W. Jaffe, B. Miller, J. Yetter (1992: Hewlett Packard. Proceedings of IEEE Hot Chips IV)
2. Multiprocessor Features in a PA-RISC Processor Interface Chip (.pdf) T. Alexander et al (1992: Hewlett Packard. Proceedings of IEEE Hot Chips IV)
3. Évolution des gammes de processeurs MIPS, DEC Alpha, PowerPC, SPARC, x86 et PA-RISC (PDF) André Seznec and Thierry Lafage (INRIA: June 1997)

2.2.4 PA-7100LC (PCX-L) processor

Overview

The PA-7100LC is a 32-bit PA-RISC processor from HP introduced in 1994, designed as a single-chip solution for low-cost systems with the performance of comparable workstations and servers. The CPU core is close to the earlier PA-7100 processor and was integrated with FPU, MIOC, first-level cache, onto a single chip with direct GSC main bus attachment.

The successor of the PA-7100LC is the similar and improved PA-7300LC processor, released two years later.

Details

- PA-RISC version 1.1c, 32-bit architecture, 2-way superscalar
- Three functional units: 2 integer ALUs, 1 FPU
- Five-stage pipeline
- 3-instruction queue
- Hardware *static* branch prediction
- TLB: 64-entry fully associative; BTLB: 8-entry
- Cache L1 1 KB on-chip I L1 instruction cache, prefetch from off-chip I cache
- Cache L1 up to 2 MB off-chip unifiede, direct mapped, 480-600 MB/s bandwidth
- Memory and I/O controller MIOC integrated on die, direct memory interface
- Support for bi-endian load-store operations
- MAX-1 multimedia extensions for multimedia applications, like MPEG decoding
- GSC bus interface
- Up to to 100 MHz, clock speed
- 14.2×14.2 mm^2 die, 900,000 FETs, 0.75µ, 3-layer aluminium process packaged in a 432-pin PGA

Only one of the two integer ALUs is able to handle loads, stores and shifts, these operations can only be paired with simple math operations, like integer addition or multiplication. Both units can handle branch operations. Used in

- HP 9000 712, 715, 725, 743i, 748i VME workstations and V743 VXI workstation
- HP 9000 D200, D210, D300, D310 servers
- HP 9000 E25, E35, E45, E55 servers
- Hitachi 3050RX 225, 235, 255, 535, e9000V V715, V715Tiny, VE25, VE35, VE45, VE55 workstations
- SAIC Galaxy 1100 portable workstations

References

1. PA7100LC ERS (External Reference Specification) (.pdf) Hewlett-Packard Company (1999)
2. The PA 7100LC Microprocessor: A Case Study of IC Design Decisions in a Competitive Environment Mick Bass et al (April 1995: Hewlett-Packard Journal. Accessed May 2009)
3. Design methodologies for the PA 7100LC microprocessor (.pdf) Mick Bass et al (April 1995: Hewlett-Packard Journal. Accessed May 2009)

2.2.5 PA-7200 (PCX-T') processor

Overview

The PA-7200 completely revised the PA-7100 processor core, leveraging only the FPU in its release in early 1995. Being a two-way superscalar processor, the PA-7200 can dispatch and execute two separate instructions at a time to its functional units. In contrast to the PA-7100 it has two separate integer ALUs and thus can execute two ALU integer operations simultaneously. Other changes include a redesigned cache architecture — while retaining the general cache layout with large off-chip L1 caches at CPU clock speed — and use of the Runway processor bus, carried on to later PA-8x00 processors. The PA-7200 was targeted towards high-performance general-purpose applications, but also on specialized applications with large working sets which could take advantage of the high-bandwidth bus interface.

Details

- PA-RISC version 1.1d, 32-bit architecture, multi-processor capable, 2-way superscalar
- Three functional units: 2 integer ALUs, 1 FPU
- Five-stage pipeline
- 3-instruction queue
- Hardware *static* branch prediction
- TLB: 120-entry fully associative; BTLB: 16-entry
- Cache L1 2 KB on-chip "assist" cache, fully associative, holds 64 32-Byte cache lines
- Cache L1 up to 1 MB I and 2 MB D asynchronous SRAMs with one cycle latency
- FPU, MMU, cache controller integrated on die, memory and I/O controller separate and off-chip
- Bi-endian support
- Runway system interface, 64-bit, 120 MHz, 960 MB/s peak bandwidth
- Glueless interface to the Runway system bus for up to four-way SMP, four CPUs on same Runway processor bus
- Up to 140 MHz clock speed with 4.4 V core and 3.3 V I/O voltage
- 14.0×15.0 mm^2 die, 1,300,000 FETs, 0.55µ, 3-layer metal CMOS14A in a 540-pin ceramic PGA, 29W power at 140 MHz

Used in

- HP 9000 C100, C110 workstations
- HP 9000 D250, D260, D350, D360 servers
- HP 9000 J200, J210 workstations
- HP 9000 K100, K200, K210, K220, K400, K410, K420 servers
- Convex SPP1200/CD, SPP1200/XA, SPP1600/CD, SPP1600/XA mainframes

- Hitachi 9000V VQ200, VQ210, VR100, VR200, VR400 servers

References

1. Design of the HP PA 7200 CPU (.pdf) Kenneth K. Chan et al (February 1996: Hewlett-Packard Journal) (mirror: Design of the HP PA 7200 CPU)
2. Verification, Characterization, and Debugging of the HP PA 7200 Processor (.pdf) Thomas B. Alexander et al (February 1996: Hewlett-Packard Journal)
3. A Different Kind of RISC Dick Pountain (August 1994: BYTE Journal)
4. Interview with David Fotland, September/October 2008

2.2.6 PA-7300LC (PCX-L2) processor

Overview

The PA-7300LC is an integrated, "low-cost" PA-RISC 32-bit processor, released in mid-1996. While being a close successor to the earlier PA-7100LC, it has several enhancements:

1. Large on-chip L1 caches, in contrast to the small "assist" caches of the PA-7100LC and PA-7200.
2. Integrated L2 cache controller in the MIOC.
3. Improved bus interface with faster GSC bus variant.
4. Faster memory interface.

The then current process technologies made it possible to include a large L1 cache on the CPU die, breaking a long-standing HP tradition of large off-chip L1 caches. The PA-7300LC was the final 32-bit, PA-RISC version 1.1 CPU, later workstations and servers used 64-bit PA-RISC 2.0 processors, such as the PA-8000, being introduced in the same timeframe.

Details

- PA-RISC version 1.1e 32-bit
- Three functional units: 2 integer ALUs, 1 Floating Point unit
- 2-way superscalar
- MAX-1 multimedia extensions for multimedia applications
- 64 KB/64 KB I/D on-chip L1 caches, each two-way set associative, virtually indexed
- Cache line size of 32 Byte
- Caches have a 64-bit datapath to the execution units, 256-bit datapath to main memory
- Optional unified I/D L2 off-chip cache, up to 8192 KB
- No hashing for both I and D caches
- L2 cache is write-through, direct mapped, physically indexed and physically tagged
- Instruction prefetch buffer moved from memory controller to L1 instruction cache, thus allowing prefetch hits without penalty
- On-chip MIOC memory controller
- 96-entry unified I/D TLB
- 8-entry BTLB
- 4-entry ILAB
- GSC system interface implements GSC+ features, maximum clock frequency of 40 MHz — actual system implement from 33 MHz and 132 MB/s up to 40 MHz and 160 MB/s
- Either 64-bit or 128-bit datapath from execution units to the memory
- Up to 180 MHz frequency with 3.3 V core voltage

- 15.3×17.0 mm^2 die, 9,200,000 FETs, 0.5µ, 4-layer metal CMOS14C process in a 464-pin ceramic PGA package

Only one of the two integer ALUs is able to handle loads, stores and shifts, these operations can only be paired with simple math operations, like integer addition o multiplication. Both units can handle branch operations.

Used in

- HP 9000 744, 745, 748 VME workstations
- HP 9000 A180, A180C servers
- HP 9000 B132L, B132L+, B160L, B180L+ workstations
- HP 9000 C132L, C160L workstations
- HP 9000 D220, D230, D320, D330 servers
- RDI PrecisionBook laptop
- Hitachi 3050RX 255, 355E, 365 workstations
- HP Agilent 16600A, 16700A, 16700B, 16702A and 16702B series logic analyzers

References

1. PA7300LC ERS (External Reference Specification) (PDF, 716 KB) Hewlett-Packard Company (1996)
2. The PA-7300LC: the first "System on a Chip" (archive.org mirror) Tom Meyer (1996: Presentation for Microprocessor Forum 1995)
3. The PA 7300LC Microprocessor: A Highly Integrated System on a Chip (PDF, 50 KB) Terry W. Blanchard and Paul G. Tobin (June 1997: Hewlett-Packard Journal)

2.2.7 PA-8000 (PCX-U) processor

Overview

The PA-8000 is the first 64-bit PA-RISC 2.0 processor, and included out-of-order execution capabilities for the first time. It was released in 1996, in parallel to the 32-bit low-cost PA-7300LC processor. The PA-800 had four integer, four floating-point and dual load/store units, a large OoO dispatch window and no on-chip caches. It was the first chip to implement the 64-bit PA-RISC 2.0 architecture to support 64-bit computing, which included 64-bit wide integer registers and functional units like ALU and a flat virtual address space of 64-bit. Other extensions in the PA-8000 included fast TLB insert instructions, memory prefetch instructions, support for variable sized pages, branch prediction hinting and new floating point units (FPMAC).

A key design feature of the PA-8000 and all following PA-RISC 2.0 processors was the IRB, the Instruction Reorder Buffer, which enables the processor to perform its own instruction scheduling in hardware, independent of compiler or software technologies. The IRB is the key part for the out-of-order capabilities of the PA-8000, and can store up to 28 computation and 28 load/store instructions, tracks interdepencies between these instructions and allows execution as soon as they are ready.

All later PA-8x00 processors up to the PA-8900 include only a slightly modified PA-8000 core with various mild extensions, and later much bigger caches.

Details

- PA-RISC version 2.0, 64-bit architecture, multi-processor capable, 4-way superscalar
- Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- IRB: 56-entry instruction queue/reorder buffer
- TLB: 96-entry fully-associative dual-ported
- BTAC: 32-entry Branch Target Address Cache; BHT: 256-entry Branch History Table
- Cache L1 1 MB I and 1 MB D off-chip, in synchronous 150 MHz 1 Mb SRAMs, one cycle latency
- Caches are direct-mapped and dual-ported
- Memory and I/O controllers are external
- Bi-endian support
- MAX-2 multimedia extensions subword arithmetic for multimedia applications
- Runway system bus, 120 MHz, 64-bit, about 960 MB/s peak bandwidth
- Up to 180 MHz, clock speed with 3.3 V core voltage
- 17.7×19.6 mm^2 die, 4,500,000 FETs, 0.5µ, 5-layer metal CMOS packaged in a 1,085-pin flip-chip LGA package

Used in

- HP 9000 C160, C180 workstations

- HP 9000 D270, D280, D370, D380 servers
- HP 9000 J280, J282 workstations
- HP 9000 K250, K260, K450, K460 servers
- HP 9000 R380 servers
- HP 9000 T600 mainframes
- HP/Convex SPP2000 (S-Class/X-Class) mainframes
- NEC TX7/D280, TX7/K370, TX7/P590 servers
- Stratus Continuum 628, 1228 mainframes

References

1. Advanced Performance features of the 64-bit PA-8000 (archive.org mirror) Doug Hunt (1995: IEEE CompCon 5)
2. PA-8000 Combines Complexity and Speed (archive.org mirror) Linley Gwennap (1994: Microprocessor Report, Volume 8 Number 15)
3. Four-Way Superscalar PA-RISC Processors (.pdf) Anne P. Scott et al (August 1997: Hewlett-Packard Journal)
4. *The HP PA-8000 RISC CPU A High Performance Out-of-Order Processor* (.pdf) [link gone] Ashok Kumar (August 1996: IEEE Hot Chips VIII)

2.2.8 PA-8200 (PCX-U+) processor

Overview

The PA-8200 is a 64-bit PA-RISC processor from HP that extended the original 64-bit PA-8000 soon after its release. Several aspects of the PA-8000 were improved with the PA-8200, released in 1997: branch prediction, TLB miss rates and cache sizes.

The PA-8200 should offer improved performace, compatibility with existing applications and short time to market. The availability of new 4 Mb SRAMs with faster access times allowed for increased CPU speed and larger caches. Smaller changes include an increase to the BHT and TLB as "high benefit, low risk" improvements.

Details

- PA-RISC version 2.0, 64-bit architecture, multi-processor capable, 4-way superscalar
- Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- IRB: 56-entry instruction queue/reorder buffer
- TLB: 120-entry fully-associative dual-ported
- BTAC: 42-entry Branch Target Address Cache; BHT: 1024-entry Branch History Table
- Cache L1 2 MB I and 2 MB D off-chip, in synchronous 200 MHz 4 Mb SRAMs, one cycle latency
- Caches are direct-mapped and dual-ported
- Memory and I/O controllers are external
- Bi-endian support
- MAX-2 multimedia extensions subword arithmetic for multimedia applications
- Runway system bus, 120 MHz, 64-bit, about 960 MB/s peak bandwidth
- Up to 300 MHz, clock speed with 3.3 V core voltage
- 0.5µ, 5-layer metal CMOS

Used in

- HP 9000 C200, C240 workstations
- HP 9000 D390 servers
- HP 9000 J2240 workstations
- HP 9000 K370, K380, K570, K580 servers
- HP 9000 R390 servers
- HP 9000 V2200, V2250 mainframes
- HP 9000 NEC TX7/V2200 mainframes

References

1. Four-Way Superscalar PA-RISC Processors (PDF, 190 KB) Anne P. Scott et al (August 1997: Hewlett-Packard Journal)
2. HP Pumps Up PA-8x00 Family (archive.org mirror) Linley Gwennap (October 1994: Microprocessor Report, Volume 10 Number 14). [Article reprint for cpu.hp.com]
3. HP's Latest PA-RISC Microprocessor Evolution Enables 50 Percent Application Performance Boost Hewlett-Packard (October 1996: HP press release). [Article mirror for hp.com]

2.2.9 PA-8500 (PCX-W) processor

Overview

The PA-8500 64-bit PA-RISC processor is the direct evolution of the PA-8000 and PA-8200 processors, leveraging their processing core but implementing large on-die L1 caches. Introduced in September 1998, the PA-8500 marked a break with the long-standing HP tradition of keeping large L1 caches off-chip. (The two years older PA-7300LC also included on-chip L1 caches, albeit much smaller). There were no other significant changes to the processing core, besides small increases to the TLB and BHT.

Details

- PA-RISC version 2.0, 64-bit architecture, multi-processor capable, 4-way superscalar
- Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- IRB: 56-entry instruction queue/reorder buffer
- TLB: 160-entry fully-associative dual-ported
- BTAC: 32-entry Branch Target Address Cache; BHT: 2048-entry Branch History Table
- Cache L1 0.5 MB I and 1 MB D on-chip, each 4-way set associative
- Memory: up to 1 TB memory supported with 40-bit physical addresses
- Memory and I/O controllers are external
- Bi-endian support
- MAX-2 multimedia extensions subword arithmetic for multimedia applications
- Runway+ system bus, 125 MHz, 64-bit, DDR, about 2 GB/s peak bandwidth
- Up to 300 MHz, clock speed with 3.3 V core voltage
- 21.3×22.0 mm^2 die, 140,000,000 FETs, 0.25µ(micron), 5-layer metal CMOS packaged in a 544-pin LGA package

Used in

- HP 9000 A400-44 (rp2400), A500-44 (rp2450) servers
- HP 9000 B1000, B2000 workstations
- HP 9000 C360, C3000 workstations
- HP 9000 J5000, J7000 workstations
- HP 9000 L1000-36, L1000-44 (rp5400), L2000-36, L2000-44 (rp5450) servers
- HP 9000 N4000-36, N4000-44 (rp7400) servers
- HP 9000 V2500 mainframes
- Stratus Continuum 419, 429, 616S, 616, 619, 629, 1219, 1229 mainframes

References

- HP Pumps Up PA-8x00 Family (archive.org mirror) Linley Gwennap (October 1994: Microprocessor Report, Volume 10 Number 14). [Article reprint for vanished cpu.hp.com]
- A 500 MHz 1.5 MByte Cache with On-Chip CPU (PDF, 141 KB) Jonathan Lachman and J. Michael Hill (1997: ISSCC).
- PA-8500: The Continuing Evolution of the PA-8000 Family (archive.org mirror) Gregg Lesartre and Doug Hunt (1997: Proceedings of CompCon, IEEE CS Press). [Article reprint for vanished cpu.hp.com]

2.2.10 PA-8600 (PCX-W+) processor

Overview

The PA-8600 is a slightly modified PA-8500 in a new manufacturing process to achieve higher clock speeds. Released in January 2000, the PA-8600 was a PA-RISC 2.0 64-bit processor, and used as upgrade in many HP 9000 servers and workstations.

Details

- PA-RISC version 2.0, 64-bit architecture, multi-processor capable, 4-way superscalar
- Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- IRB: 56-entry instruction queue/reorder buffer
- TLB: 160-entry fully-associative dual-ported
- BTAC: 32-entry Branch Target Address Cache; BHT: 2048-entry Branch History Table
- Cache L1 0.5 MB I and 1 MB D on-chip, each 4-way set associative
- Memory: up to 1 TB memory supported with 40-bit physical addresses
- Memory and I/O controllers are external
- Bi-endian support
- MAX-2 multimedia extensions subword arithmetic for multimedia applications
- Runway+ system bus, 125 MHz, 64-bit, DDR, about 2 GB/s peak bandwidth
- Up to 550 MHz, clock speed with 2.0 V core voltage
- 21.3×22.0 mm^2 die, 140,000,000 FETs, 0.25µ(micron), 5-layer metal CMOS packaged in a 544-pin LGA package

Used in

- HP 9000 A400-5X (rp2400), A500-5X (rp2450) servers
- HP 9000 B2000 (some), B2600 workstations
- HP 9000 C3600 workstations
- HP 9000 J5600, J6000, J7600 workstations
- HP 9000 L1000-5X (rp5400), L2000-5X (rp5450), L1500-5X (rp5430), L3000-5X (rp5470)
- HP 9000 N4000-5X (rp7400) servers
- HP 9000 V2600 mainframes
- HP 9000 Superdome mainframes
- NEC NX7000/L1000, NX7000/L2000, NX7000/L3000 servers
- Stratus Continuum 439, 449, 651-2, 652-2, 1251-2, 1252-2 mainframes

2.2.11 PA-8700 (PCX-W2) processor

Overview

The PA-8700 processor is an 64-bit HP PA-RISC processor from HP, released in 2001 building on an enhanced PA-8500 core with several modifications. As with other PA-8x00 processors, the logic core is close to the original PA-8000 from 1997. The PA-8700 used significant larger on-chip L1 caches and TLB while switching to a new manufactoring process at IBM helped increase the clock speed. At its time it was one of the largest available commercial processors and one of the first manufactured in Silicon On Insulator.

Details

- PA-RISC version 2.0, 64-bit architecture, multi-processor capable, 4-way superscalar
- Ten functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- IRB: 56-entry instruction queue/reorder buffer
- TLB: 240-entry fully-associative dual-ported
- BTAC: 32-entry Branch Target Address Cache; BHT: 2048-entry Branch History Table
- Cache L1 0.75 MB I and 1.5 MB D on-chip, 4-way set associative, in independent 0.75 MB banks.
- Memory: up to 16 TB memory supported with 44-bit physical addresses
- Memory and I/O controllers are external
- Bi-endian support
- MAX-2 multimedia extensions subword arithmetic for multimedia applications
- Runway+ system bus, 125 MHz, 64-bit, DDR, about 2.0 GB/s peak bandwidth
- Up to 750 MHz, 875 MHz on the PA-8700**+** clock speed with 1.5 V core voltage
- 16.0×19.0 mm^2 die, 186,000,000 FETs, 0.18µ, 7-layer Silicon-on-Insulator CMOS packaged in a 544-pin LGA package

Used in

- HP 9000 A400-6X (rp2430), A500-6X, A500-7X (rp2470), rp2405 servers
- HP 9000 C3650, C3700, C3750 workstations
- HP 9000 J6700 workstations
- HP 9000 L1500-6X, L1500-7X, L1500-8X (rp5430), L3000-6X, L3000-7X, L3000-8X (rp5470) servers
- HP 9000 N4000-6X, N4000-7X (rp7400) servers
- HP 9000 N4000-6X, N4000-7X, N4000-8X (rp7405, rp7410) servers
- HP 9000 Superdome mainframes

References

1. A 900 MHz 2.25 MByte Cache with On Chip CPU (PDF, 119 KB) J. Michael Hill and Jonathan Lachman (2000: ISSCC)
2. PA-RISC 2.0 Architecture (.pdf) Hewlett-Packard Company (1995)
3. HP taps new foundry for PA-RISC processors, EE Times, August 2001

2.2.12 PA-8800 (Mako)

Overview

The dual-core PA-8800 Mako processor, introduced in 2004, is a PA-RISC 2.0 64-bit processor from HP that integrated two seperate PA-8700 cores on a single die with very large off-die L2 caches. The clock speed was only increased slightly, while the processor bus interface was redesigned to use the Itanium 2 bus. Mako was supposed to breathe fresh life in the PA-RISC line, though it had strong internal competition from the Itanium line, a VLIW development from HP and Intel, and was not marketed much. Most systems supporting PA-8800s use the HP zx1 chipset and could be hardware-upgraded to use Itanium 2 IA64 processors.

Details

- PA-RISC version 2.0, 64-bit architecture, multi-processor capable, 4-way superscalar
- Two cores and ten functional units per core: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- IRB: 56-entry instruction queue/reorder buffer
- TLB: 240-entry fully-associative dual-ported per core
- BTAC: 32-entry Branch Target Address Cache; BHT: 2048-entry Branch History Table per core
- Cache L1 0.75 MB I and 0.75 MB D per core on-chip, 4-way set associative
- Cache L2 32 MB off-chip, four 8 MB DDR-ESRAM chips, 300 MHz clock, each 2.7 GB/s bandwidth
- Cache L2 is shared between the cores, L2 controller is on-chip
- Memory: up to 16 TB memory supported with 44-bit physical addresses
- Memory and I/O controllers are external
- Bi-endian support
- MAX-2 multimedia extensions subword arithmetic for multimedia applications
- Itanium 2 processor bus, 200 MHz clock, 128-bit, 6.4 GB/s bandwidth
- Up to 1 GHz clock speed with 1.5 V core voltage
- 23.6×15.5 mm^2 die, 300,000,000 FETs, 0.13µ, 8-layer Silicon-on-Insulator CMOS fabbed by IBM

Used in

- HP C8000 workstations
- HP 9000 L1500-9X (rp5430), L2000-9X (rp5450) servers
- HP 9000 N4000-9X (rp7405, rp7410) servers
- HP 9000 rp3410, rp3440 servers

- HP 9000 rp4410, rp4440 servers
- HP 9000 rp7420 servers
- HP 9000 rp8400, rp8410, rp8420 servers
- HP 9000 Superdome mainframes

References

- HP's Mako Processor (PDF, 1.4 MB) David J. C. Johnson (2001: Microprocessor Forum).

2.2.13 PA-8900 processor

Overview

The PA-8900 is a slightly tweaked PA-8800 PA-RISC processor with a doubled L2 cache and higher clock speed, released by HP in 2005 only one year after the PA-8800 as the last PA-RISC processor in its lineup. After HP dropped its line of Itanium workstations the PA-8900-powered C8000 were one of the last HP-UX workstations.

Information on the PA-8900 is limited, as was apparent distribution in the market.

Details

- PA-RISC version 2.0, 64-bit architecture, multi-processor capable, 4-way superscalar
- Two cores and ten functional units per core: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- IRB: 56-entry instruction queue/reorder buffer
- TLB: 240-entry fully-associative dual-ported per core
- BTAC: 32-entry Branch Target Address Cache; BHT: 2048-entry Branch History Table per core
- Cache L1 0.75 MB I and 0.75 MB D per core on-chip, 4-way set associative
- Cache L2 64 MB off-chip
- Cache L2 is shared between the cores, L2 controller is on-chip
- Memory: up to 16 TB memory supported with 44-bit physical addresses
- Memory and I/O controllers are external
- Bi-endian support
- MAX-2 multimedia extensions subword arithmetic for multimedia applications
- Itanium 2 processor bus, 200 MHz clock, 128-bit, 6.4 GB/s bandwidth
- Up to 1.1 GHz clock speed with 1.5 V core voltage
- 23.6×15.5 mm^2 die, 317,000,000 FETs, 0.13µ, 8-layer Silicon-on-Insulator CMOS

Used in

- HP 9000 rp3410, rp3440 servers
- HP 9000 rp4410, rp4440 servers
- HP 9000 rp7440, rp8440 servers
- HP C8000 workstations
- HP 9000 L1500-9X (rp5430), L2000-9X (rp5450) servers
- HP 9000 N4000-9X (rp7405, rp7410) servers

- HP 900 Superdome mainframes

References

- Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers (PDF, 700 KB) Hewlett-Packard (2005).

2.2.14 Other PA-RISC processors

Several other third-party processor designers implemented PA-RISC processors and solutions both for workstation and server use (Hitachi) but also for embedded systems of the 1990s like set-top boxes, TVs and for device controllers such as printers.

Table 2.3: Other PA-RISC processors overview

CPU	**ISA**	**Release**	**Clock**	**Cache**	**Bus**	**Super scalar**	**Units**	**Controllers** *on-chip*
Hitachi PA/50L	PA 1.1 32-bit	1993	33MHz	12KB	?	1-way	1 Integer 1 Floating Point	
Hitachi PA/50M	PA 1.1 32-bit	1993	60MHz	12KB	?	1-way	1 Integer 1 Floating Point	
Hitachi HARP-1	PA 1.1 32-bit	1994	150MHz	24KB 1MB L2	?	2-way	2 Integer 1 Floating Point *(Vector)*	
Winbond W89K	PA 1.1 32-bit	1994	33/66MHz	4KB	Intel 486	1-way	1 Integer	none?
Winbond W90210 W90215	PA 1.1 32-bit	1997	33/66MHz	12KB	Intel 486	1-way	1 Integer *MAX-1*	DRAM DMA PCI I/O
Winbond W90220 W90221	PA 1.1 32-bit	1999	150MHz	8KB	Intel 486	1-way	1 Integer 1 MAC(DSP) *MAX-1*	DRAM DMA PCI IDE I/O VGA (W90221) TV (W90221)
Oki OP32	PA 1.1 32-bit	1994	33MHz	?	?	1-way	1 Integer	DRAM DMA
Amiga Hombre	PA 1.1 32-bit	1995	125MHz	?	64-bit	1-way	1 Integer	Memory DMA PCI I/O VGA audio Copper Blitter

Hitachi PA/50L and PA/50M processors

The Hitachi PA/50 was a family of PA-RISC 1.1 processors designed and manufactured by Hitachi, released in 1993. Two designs were developed: **M**, with around 100 MIPS, and **L**, "low-cost" , with around 55 MIPS. They were used as personal workstation processors and high-end embedded controllers and integrated a set of features previously not available at that time in other PA-RISC processors like on-chip caches, data-prefetching, a power-saving mode and SDRAM support.

- PA-RISC version 1.1 32-bit

- Built-in, pipelined FPU
- L1 I: 8 KB, 2-way set-associative, 32-byte blocks
- L1 D: 4 KB, 2-way set-associative, 32-byte blocks, copy-back
- L1 caches are on-chip
- Uncacheable memory (per page)
- TLB: I/D 32/64-entry, 2-way set, 4K-page, each +2 additional block entries
- BTLB (256 KB-32 MB)
- Seven 32-bit shadow registers for fast interrupts
- Data-prefetching
- Non-blocking cache
- Power-saving mode, reducing frequency to 1/8
- Support for SDRAM
- PA/50L: Up to 33 MHz frequency with 3.3 V core voltage
- PA/50M: Up to 60 MHz frequency with 5.0 V core voltage
- 11.5×12.0 mm^2 die, 1,280,000 FETs, 0.6µ(micron), 3-layer metal CMOS packaged in a 160-pin plastic QFP package

Used in

- Hitachi 3050RX 100C, 200 workstations

Hitachi HARP-1 processor

The Hitachi HARP-1 is a PA-RISC version 1.1 compatible CPU from Hitachi, introduced in June 1994. It is apparently a larger and faster version of the PA/50 processor, however . not much information is available on either processor.

The HARP-1**E** variant supposedly includes ("pseudo") vector processing modifications/add-ons and was used in Hitachi vector/supercomputers. It seems the L1 cache was increased to 16 KB/16 KB instruction/data.

- PA-RISC version 1.1 32-bit
- Three functional units: two integer ALUs and one floating point unit and two shift-merge units
- Six-stage pipeline
- Built-in, pipelined FPU
- Built-in memory controller Memory Interface Unit, MIU
- 2-way superscalar
- L1 I cache: 8 KB, 1-way set-associative, 32-byte blocks
- L1 D cache: 16 KB, 2-way set-associative, 32-byte blocks, copy-back

- L1 caches are on-chip
- L2 I/D 512/512 KB, off-chip
- TLB: I/D 128/128-entry, 1-way set
- Some say a second level TLB was included
- L2 Cache bus: 128-bit data path to L2 caches with ECC
- Processor bus: 64-bit data path to main memory and I/O
- Up to 150 MHz frequency with 3.3 V core voltage, 17W power dissipation at 120 MHz
- 16.2×16.5 mm^2 die, 2,800,000 FETs, 0.5µ3-layer aluminium + 1-layer tungsten BiCMOS, packaged in 595-pin PGA

Used in

- Hitachi SR2201 supercomputer (HARP-1**E**)
- Probably others

Winbond W89K processor

The Winbond W89K is an embedded 32-bit PA-RISC controller chip, pin-compatible with the then-popular Intel 80486DX, introduced in Spring 1994. It could be used as a drop-in replacement in mid-1990s PCs together with Winbond BIOS replacement chips. Rationale was to allow hardware developers utilize existing 486DX mainboards and components for a shorter product development process. The W89K is a level 0 PA-RISC 1.1 implementation: a 32-bit PA-RISC processor without virtual addressing.

- PA-RISC version 1.1 32-bit
- Level 0 implementation, no virtual addressing: no MMU
- Five-stage pipeline
- One functional unit: one 32-bit integer ALU
- 2 KB/2 KB I/D on-chip L1 caches
- 80486 Intel bus interface
- 33 MHz and 66 MHz clock speeds were available, with the latter apparently having been achieved with a clock-doubling also used in the Intel's 80486DX/2
- On-chip JTAG support
- 14.3×14.3 mm^2 die, 1,100,000 FETs, 0.8µ, 3-layer metal CMOS

Winbond W90210/215 processor

Shortly after the W89K embedded controllers Winbond introduced more sophisticated PA-RISC processors in Fall 1997 with the W90K line of embedded controllers. The W90210F still was 32-bit PA-RISC 1.1 but integrated many external I/O components on the chip — DRAM and DMA controllers, a PCI bridge and various I/O ports. As its predecessor, the W90210F was a level 0 PA-RISC 1.1

implementation without virtual addressing. It was apparently used in various "Internet appliances": set-top boxes, TV sets, DVD players, PDAs, VoIP devices, and for industrial automation. The W90215 is identical to the W90210 but did not include license rights for the embedded operating system and was thus cheaper.

- PA-RISC version 1.1 32-bit
- Level 0 implementation no virtual addressing: no MMU
- Five-stage pipeline
- One functional unit: one 32-bit integer ALU
- L1 I cache: 4 KB, direct mapped, 32-byte blocks, 256 entries
- L1 D cache: 8 KB, 2-way set-associative, 32-byte blocks, 2×64 entries, write-back
- MAX-1 multimedia extensions for multimedia applications, like MPEG decoding
- 80486 Intel bus interface
- DRAM controller
- ROM/FLASH interface
- DMA controller 2-channel 8-bit
- PCI bridge
- Two serial ports
- Parallel port
- 33 MHz and 66 MHz clock speeds
- 208-pin PQF package

Winbond W90220 and W90221 processors

The W90220F is, as its predecessor W90210, a 32-bit PA-RISC 1.1 design without MMU but integrated many external I/O components on the chip — DRAM and DMA controllers, PCI bridge, IDE channels, I/O ports and, on the W90221, a graphics/TV chip. Released in Spring 1999, it had the same target systems of set-top boxes and internet appliances. The sucessor W90221 is apparently similar, with higher clock speed, integrated (S)VGA and TV controller

- PA-RISC version 1.1 32-bit
- Level 0 implementation, no virtual addressing: no MMU
- Six-stage pipeline
- Two functional units: one 32-bit integer ALU and one 32-bit multiply-accumulate MAC module, for DSP purposes, can be used as two 16-bit modules too
- L1 I cache: 4 KB, direct mapped, 32-byte blocks, 256 entries
- L1 D cache: 4 KB, 4-way set-associative, write-back or write-through
- MAX-1 multimedia extensions for multimedia applications, like MPEG decoding
- 80486 Intel bus interface

- ◈ Hardware *dynamic* branch prediction
- ◈ 256-entry branch-target-buffer BTAC
- ◈ Memory controller supports DRAM, EDO-DRAM and SRAM; W90221 additionally SDRAM
- ◈ ROM/FLASH interface
- ◈ DMA controller 2-channel 8-bit
- ◈ IDE I/O controller four 16-bit channels
- ◈ W90221: VGA and TV controller W9971
- ◈ PCI bridge
- ◈ Two serial ports
- ◈ Parallel port
- ◈ Serial ICE port
- ◈ Up to 150 MHz clock speed at 3.3 V/5 V I/O and 3.3 V core
- ◈ W90221: 133 MHz clock speed with apparently 3.3 V at both I/O and core
- ◈ 0.35µsingle-poly-triple-metal CMOS
- ◈ 208-pin PQF package

Oki OP32 processor

Oki Semiconductor OP32/50N was introduced in 1994 as an embedded controller, based on a 32-bit PA-RISC design with integrated DRAM and DMA controllers. The chip was targeted at laser printers, Fax machines, X-Terminals and the Telecom and Automotive markets.

- ◈ PA-RISC version 1.1 32-bit
- ◈ 33 MHz frequency
- ◈ 14.3×14.3 mm^2 die, 1,100,000 FETs, 0.8µ, 3-layer metal CMOS

2.2.15 Amiga Hombre processor

Between 1992 and 1994, Commodore designed a new graphics chipset to power Amiga computers based on HP PA-RISC, called Hombre. The development effort apparently included HP and was based on a PA-RISC core to be available for 1995 production for a "CD-based Game Machine" , cable TV, MPEG and as a PCI-based graphics accelerator. The Hombre processor design was to be implemented in two chips:

- ◈ CPU chip (Nathaniel) with 32-bit PA-RISC core: RISC integer core based on PA-7150 at 125MHz, DMA interface, audio and CD interfaces, system, display and PCI buses
- ◈ Video chip (Natalie) with graphics functions and buses
- ◈ Both were targeted for 0.6µ, 3-level metal CMOS in 3.3 V in 304-PQFP
- ◈ 50MHz system bus, 64-bit wide

The CPU core was 32-bit PA-RISC 1.1, Integer-only with a 5-stage pipeline and 64-bit datapath

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2.3 PA-RISC Architecture

This is partially old content, from early 2002/2003.

2.3.1 Precision Architecture RISC

PA-RISC is Hewlett Packard's Reduced Instruction Set Computing (RISC) architecture from the 1980s and an offspring from active HP research and development undertakings from that time. The aim of the Precision Architecture was to replace 16-bit stack-based CPUs in HP 3000 servers and Motorola 680x0 CPUs in HP's Unix systems with a common system architecture.

An earlier commercial design from HP from the early 1980s was the HP FOCUS architecture.

Overall PA-RISC was a rather conservative RISC design for that time:

- The instruction set is implemented in hardware and not microcoded.
- Instruction size is of fixed length — one word (32-bit).
- Only three addressing modes: long/short displacement and indexed.
- Only load/store operation access the memory, computational instructions do not.
- Many simple and frequently used instructions execute in just one cycle, more complex computation are assigned to assist processors or software algorithms.

Compared to other RISC architectures original PA-RISC was rather unspectacular — it had fewer features but remained always at competitive speeds, especially in Floating Point and multiprocessing. HP was the first to include multimedia extension in commercially available microprocessors, MAX-1 in the PA-7100LC and MAX-2 64-bit in the PA-8000, which allowed vector operations on two or four 16-bit subwords in 32-bit or 64-bit integer registers.

PA-RISC 1.0

The original PA-RISC 1.0 architecture was 32-bit and included a single instruction/data bus. PA-RISC later on moved to a Harvard-style architecture with seperate instruction and data buses.

PA-RISC 1.0 has thirty-two 32-bit integer general purpose registers (GR0-GR31), seven shadow registers (SR0-SR6) for fast-interrupts and thirty-two 64-bit Floating Point registers for the FPU, which also could be combined to 64×32-bit and 16×128-bit. The FPU is able to execute a Floating Point instruction simultaneously to the ALU.

The original addressing was 48-bit wide, it was later on expanded to 64-bit (with the introduction of the PA-8000 line).

PA-RISC 1.1

The PA-RISC architecture was extended to version 1.1 with the PA-7000 processor in 1991. The major change in PA-RISC 1.1 was the inclusion of a MMU (memory management unit), that enabled PA-RISC computers to use virtual memory. From the the second PA-RISC 1.1 processor, the PA-7100 onward all processors implement superscalar instruction execution — the ability to execute multiple instructions simultaneously.

The 32-bit PA-RISC 1.1 processors are up to two-way superscalar, later 64-bit processors up to four-way. Other significant developments in PA1.1 include the PA-7100LC and PA-7300LC processors (**LC** for low cost) , which integrated the memory and I/O controller onto the processor die, on the PA-7300LC additionally the cache controller and first-level cache.

PA-RISC 2.0

In 1996 the 64-bit redesign of PA-RISC was introduced with the PA-RISC 2.0 PA-8000 processor. The architectural changes were rather intrusive but stayed compatible with 32-bit PA-RISC 1.1. On a side note, the PA-RISC 2.0 and the PA-8000 were introduced *before* the last 32-bit PA-RISC processor — the PA-7300LC — shipped.

Main changes and features of PA-RISC 2.0 include:

- All registers and functional units extended to 64-bit
- Virtual address space extended to 64-bit
- Physical address space is 40-bit on PA-8000 to PA-8600 (for 1 TB of addressable physical memory) and 44-bit (16 TB memory) on PA-8700 and later
- Out-of-Order (OoO) execution capability with the IRB *(Instruction Reorder Buffer)*, which stores up to 28 computation and 28 load/store instructions and reorders and prepares the for execution on the fly. It tracks interdependecies and branch prediction outcomes as well. The IRB is *the* key part in the OoO execution capability of PA-RISC 2.0.
- FPMAC (*Floating Point Multiply Accumulate*) units

The later PA-8x00 processors of the 2000s did not introduce significant changes to the architecture or logic, besides higher integration of large L1 caches in the PA-8600 and dual-core PA-8800 and PA-8900. The processors after the PA-8000 were mostly redesigns and extensions of that processor core.

Post-PA-RISC

From the mid-1990s on a parallel track to PA-RISC 2.0 development HP joined Intel in developing the VLIW Itanium architecture from its own R&D projects, called EPIC, which resulted in the Intel/HP IA64 architecture.

Since the early-2000s HP sold two lines of Unix computers and servers in parallel — PA-RISC 2.0 and Itanium. These competing designs were apparent in the Integrity servers — with the rp servers (PA-RISC) and rx servers (Itanium).

These post-PA-RISC designs were not the success many hoped and HP after the turn of the century switched to standard Intel x86 fare.

Pre-PA-RISC

The predecessor of PA-RISC in the early 1980s was the HP FOCUS architecture from the HP 9000 Series 500. FOCUS was a stack architecture, with 230 instructions both 32 bits and 16 bits wide, a segmented memory model, and no general purpose programmer-visible registers. There are thirty-nine 32-bit registers in the CPU hardware, thirty-one internal 32-bit general purpose registers, two 32-bit ALU registers, and others.

2.3.2 Floating Point Unit (FPU)

The *Floating Point Unit* is an assist processor logically added to a system to improve the performance on floating-point operations. The processor can be on a seperate chip (*e.g.,*PA-7000) or integrated onto the central CPU die (all PA-RISC CPUs upwards). The FPU executes special floating point instruction to perform arithmetic on its own set of independent registers (*register file*) and to move data between its own registers and the system's lower memory hierarchy. The FPU execution stage is pipelined. All PA-RISC FPUs contain thirty-two 64-bit registers, which can also be used as sixty-four 32-bit registers and sixteen 128-bit registers.

2.3.3 Transition Lookaside Buffer (TLB)

The *Translation Lookaside Buffer* is a hardware structure doing virtual-to-physical memory address translations. The TLB takes virtual page numbers and returns the corresponding physical page number. The PA-7000 is the last PA-RISC processor to use seperate I/D TLBs, all later PA 1.1 and 2.0 CPUs use a combined TLB structure.

- PA-7000 - 96 I and 96 D entries
- PA-7100 - 120 combined entries
- PA-7100LC - 64 combined entries
- PA-7200 - 120 combined entries
- PA-7300LC - 96 combined entries
- PA-8000 - 96 combined entries
- PA-8200 (PCX-U+) - 120 combined entries
- PA-8500 (PCX-W) - 160 combined entries
- PA-8600 (PCX-W+) - 160 combined entries
- PA-8700 (PCX-W2) - 240 combined entries
- PA-8800 - 2×240 combined entries
- PA-8900 - 2×240 combined entries

Hitachi's PA-RISC 1.1 derivates also used split TLBs:

- Hitachi PA/50 - 32 I and 64 D entries
- Hitachi HARP-1 - 128 I and 128 D entries (some sources mention a second-level TLB)

Most interestingly, the older PA-RISC 1.0 processors (pre-PA-7000) have huge TLBs (even for today's standards):

- TS-1 - 4096 entries (split I/D)
- NS-1 - 4096 entries (split I/D)
- NS-2 - 16384 entries (split I/D)
- CMOS26B (PCX) - 8192 entries (split I/D)

The TLB memory on these earlier CPUs was implemented mostly off-chip/off-die via separate memory (SRAM) chips.

Translation process

- *PA 1.1*: If a virtual address has to be translated to a physical address, the corresponding TLB is searched for an entry matching the Virtual Page number. If an entry is found, the 20-bit Physical Page number, delivered by the TLB, is concatenated with the original 12-bit page offset to the build up the 32-bit absolute physical address.

TLB miss handling implementations

- *Hardware*: If the CPU implementation provides a hardware TLB miss handler, it attempts to find the virtual-to-physical translation in the *Page Table*. If successful, the translation and protection fields are inserted in the TLB. If not successful, an interruption occurs so the software miss handler can complete the translation.
- *Software*: If software TLB miss handling is implemented, a TLB miss fault interruption routine performs the translation. It inserts the translation and protection fields in the TLB and afterward restarts the interrupted routine, in which the TLB miss occurred.

2.3.4 Block Transition Lookaside Buffer (BTLB)

Similar to the TLB, the BTLB provides virtual-to-physical address translations. The *BTLB* however maps large address ranges rather that single pages as the TLB. These large address ranges are *block translations* and therefore stored in the *Block Translation Lookaside Buffer*. These block translations are useful for virtual address ranges that do not get paged in or out.

BTLBs were only implemented on 32-bit PA-RISC processors (PA-7x00), 64-bit PA-RISC instead implemented variable page sizes, thus any entry can be of >4k mapping.

2.3.5 Superscalar execution

Overview

A *superscalar* processor implementation decodes, dispatches and executes multiple instructions per cycle if dependencies between the instructions permit. This is possible if the instruction stream contains independent instructions. Superscalarity can be gained from a decoupled floating point unit (FPU) which executes floating point operations indepently from the integer ALU. More complicated variations allow for parallel load/store operations, integer calculations and so on, which need a more complex CPU design that analyzes the instructions/branches.

Every PA-RISC processor from the PA-7100 on implements superscalar execution. Instructions proceed together through the execution pipeline, which is called *instruction bundling*. The superscalar execution is functionally transparent to the software, the effects of any given instruction are the same whether it was executed as part of a *bundle* or alone. Bundling rules are applied at run-time by the hardware; optimal performance may only be gained by proper ordering of the instructions so the processor can use its full superscalar potential.

Several kinds of restrictions are placed upon the instruction bundling in PA-RISC:

- Functional unit contention
- Data dependency restrictions

- ◈ Control flow restrictions
- ◈ Special instruction restrictions

For bundling purposes instructions are divided into classes:

Table 2.4: PA-RISC superscalar instruction classes

Class	Description
FLOP	Floating point operation
LDST	Loads and stores
ALU	Integer ALU
MM	Shifts, extracts, deposits
NUL	Might nullify successor
BV	Branch Vectored (BV) local, Branch (BE) external
BR	Other branches
FSYS	FTEST and FP status/exception
SYS	System control instructions

PA-7100 superscalar capabilities

The PA-7100 is two-way superscalar with one integer ALU and one FPU.

Allowed bundles

Table 2.5: PA-7100 allowed instruction bundles

First instruction	Second instruction
ALU	+ FLOP
LDST	+ FLOP
FLOP	+ ALU/LDST/Branch

PA-7100LC/PA-7300LC superscalar capabilities

These are 2-way superscalar processor implementations with two integer ALUs and one FPU. Notably only one of the two ALUs is capable to handle loads, stores and shifts.

Allowed bundles

Table 2.6: PA-7100LC/PA-7300LC allowed instruction bundles

First instruction	Second instruction
FLOP	+ LDST/ALU/MM/NUL/BV/BR
LDST	+ FLOP/ALU/MM/NUL/BR
ALU	+ FLOP/LDST/ALU/MM/NUL/BR/FSYS
MM	+ FLOP/LDST/ALU/FSYS
NUL	+ FLOP
SYS	Never bundled

Besides from these bundles, *LDST + LDST* bundles are under certain circumstances also possible. These are then called *double word load/store*.

Data dependencies

Several kinds of instructions cannot be bundled together because of inter-instruction data dependencies:

- An instruction that modifies a register will not be bundled with another instruction that takes this register as operand.
  Exception: a *FLOP* can be bundled with a FP store of the *FLOP*'s result register.
- A FP load to one word of a doubleword register will not be bundled with a *FLOP* that uses the other doubleword of this register.
- A *FLOP* will not be bundled with a FP load if both instructions have the same target register.
- An instruction that could set the carry/borrow bits will not be bundled with an instruction that uses carry/borrow bits.

Control Flow

- An instruction which is in the delay slot of a branch is never bundled with other instructions.
- An instruction which is at an odd word address and executed as a target of a taken branch is never bundled.
- An instruction which might nullify its successor is never bundled with this successor. Only if the successor is a *FLOP* instruction this bundle is allowed.

PA-7200 superscalar capabilities

This is a 2-way superscalar processor implementation. It has two integer ALUs and one FPU. Similar to the PA-7100LC, shift-merge and test condition units are not duplicated in the second ALU. To support the superscalar capabilities one additional write port and two additional read ports were added to the general registers (GR*).

Allowed bundles

Table 2.7: PA-7100LC/PA-7300LC allowed instruction bundles

First instruction	Second instruction
FLOP	+ LDST/ALU/MM/NUL/BV/BR
LDST	+ FLOP/ALU/MM/NUL/BR
ALU	+ FLOP/LDST/ALU/MM/NUL/BR/FSYS
MM	+ FLOP/LDST/ALU/FSYS
NUL	+ FLOP

PA-8x00 superscalar capabilities

To be described.

2.3.6 Multimedia Acceleration eXtensions (MAX-1 and MAX-2)

MAX-1 (32-bit)

MAX-1 are the original multimedia extensions from the 1990s introduced with the HP PA-7100LC processor and later also the PA-7300LC. The aim from HP in its design was to enable contemporary workstations with these CPUs to provide real-time MPEG video decompression and playback at a rate of 30 frames/second without the need for a special DSP (digital signal processing) chip, not an easy feat.

The HP design process for the PA-7100LC processor in the early 1990s included for the first time multimedia benchmarks for analyzing optimizations in the instruction set design.

The actual implementation used a small set of SIMD-MIMD instructions to faciliate the application of instructions on bundled subword data. Since these instructions use the same data paths and execution units within the processor as the regular instructions, the design team termed this *intrinsic signal processing* (ISP).

Sticking to conventional RISC principles, the design team decided against adding complex special-purpose instructions to the design but opted for the elegant use of the existing facilities in the CPU, which were slightly modified to understand new, packed subword data.

In 1994, the MAX-1 extensions made their way into the final PA-7100LC product and as such were the first SIMD instructions pfound in a general microprocessor. Less than 0.2 percent of the processor silicon area had to be used for MAX-1 additions and modifications, while allowing a very significant performance boost in affected applications.

As an example, the then-highend HP 9000 735/99 workstation with a 99 MHz processes and 512 KB cache achieved 18.7 FPS at MPEG decompression benchmarks — the new entry-level 712 workstation at 60 MHz and 64 KB cache achieved 26 FPS, an impressive feat for the time an 1990s information technology.

New MAX-1 multimedia instructions include: parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average.

MAX-2 (64-bit)

With the introduction of the new 64-bit PA-RISC 2.0 architecture in 1996 HP unveiled a new set of multimedia-oriented instructions aimed at using the processor's resources more effectively for sub-word data. The basic components of the contemporary multimedia data were often represented as 8, 12 or 16-bit integers, for example audio sampling and pixel color depth. Doing arithmetic with data of this length would waste an considerable amount of the processor's execution capacities, a simple addition of 16-bit data would only use one quarter of the 64-bit wide integer units datapath. To remedy this situation, MAX allows for packing of these *subword data* into larger words near the processor's natural word width (64-bit on PA-RISC 2.0 processors) and using parallel instructions on them. An example would be four 16-bit additions by the 64-bit adder on four 16-bit packed subwords.

The basic functionality from the earlier 32-bit MAX-1 was taken over and four more instructions added for MAX-2. Additionally, due to the wider integer registers (now 64-bit) more subwords can be packed in one cycle, doubling the effective speed of these multimedia instructions. The MAX-2 multimedia instructions include (new in MAX-2 are in **bold**): parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average, **parallel shift right**, **parallel shift left**, **mix** and **permute**.

MAX-2 debuted 1996 with the PA-8000 processor and later featured on all subsequent PA-RISC 2.0 processors (PA-8x00). In contrast to contemporary multimedia extensions, MAX-2 required only very little die space (0.1 percent on the PA-8000).

2.3.7 Further reading

Selected papers and articles for further reading on the PA-RISC architecture and platform

- Hewlett-Packard Precision Architecture: The Processor (.pdf) M. Mahon et al (August 1986: Hewlett Packard Journal. Accessed May 2009)
- PA-RISC 1.1 Architecture and Instruction Set Reference Manual (.pdf) Hewlett-Packard Company (February 1994, third edition. Accessed May 2009 at PA-RISC Linux FTP)
- PA-RISC 2.0 Instruction Set Architecture (.pdf) Hewlett-Packard Company (1995. Accessed May 2009 at PA-RISC Linux FTP)
- Great Microprocessors of the Past and Present, John Bayko (June 2001/V 12.1.1: BURKS. Accessed 28 Dec 2007)
- Single Instruction Multiple Data, Multiple Instruction Multiple Data (MIMD), see for example the SIMD Wikipedia article and MIMD Wikipedia article
- Accelerating Multimedia with Enhanced Microprocessor (PDF, 2.4 MB) Discussion of the MAX-1 instructions. Ruby Lee, April 1995, IEEE Micro, Volume 15 Number 2.
- 64-bit and Multimedia Extensions in the PA-RISC 2.0 Architecture (PDF, 66 KB) New features of the 64-bit PA-RISC 2.0 architecture and overview on the MAX introduced with it. Ruby Lee and Jerry Huck, 1996, Hewlett-Packard Company.
- Subword Parallelism with MAX-2 (PDF, 1.5 MB) Discussion of the MAX-2 instructions. Ruby Lee, August 1996, IEEE Micro, Volume 16 Number 4.

2.4 PA-RISC Chipsets

Most HP PA-RISC computers used proprietary HP chipsets and system designs. Early 32-bit workstations (HP 9000/700) and servers (HP 9000/800) from the 1990s used different chipsets. Later on, the system platforms of workstations and servers moved closer and used the same chipsets.

Table 2.8: Chipsets used in PA-RISC computers

Architecture and CPUs	**Chips**	**Usage**
Early designs	SIU/SPI	CPU bridge
TS-1, NS-1, NS-2, PCX	CTB	I/O bridge
ASP/Viper	Viper	Memory and I/O controller
PA-7000, PA-7100	ASP	I/O chipset
LASI	MIOC	Memory and I/O controller
PA-7100LC, PA-7300LC	LASI	I/O chipset
	Wax	EISA bridge
	Dino	PCI bridge
	Cujo	PCI-64 bridge
U2/UTurn	MMC/SMC	Memory controller
PA-7200, PA-8000, PA-8200	U2 or UTurn	I/O controller
	LASI	I/O chipset
	Wax	EISA bridge
	Dino	PCI bridge
	Cujo	PCI-64 bridge
Astro	Astro	Memory and I/O controller
PA-8500, PA-8600, PA-8700	Elroy	Bus bridge to I/O
Stretch	DEW	CPU bridge
PA-8500, PA-8600, PA-8700	Prelude	Memory controller
	IKE	I/O controller
	Elroy	PCI-64 bridge
Cell	CC	Memory and I/O controller
PA-8700, PA-8800, PA-8900	XBC	Crossbar
	SBA	I/O controller
	Elroy	PCI-64 bridge
zx1	Pluto	I/O and memory controller
PA-8800, PA-8900	Mercury	PCI, PCI-X, AGP bridge

Chipsets were tied to specific architectures but sometimes used in different generations of computers or implementations.

Early designs: Early 32-bit PA-RISC systems of the late 1980s used custom designs based on the SIU/SPI main bus interfaces and the SMB bus. The computing and I/O units consisted of a large number of individual chips and used CIO and HP-PB I/O buses.

ASP/Viper: Computers with 32-bit PA-7000 and PA-7100 processors mostly used the ASP chipset and Viper memory controller, with VSC CPU, GSC system and SGC and EISA expansion buses.

LASI: Developed as highly-integrated chipset and system design, many LC low-cost systems with PA-7100LC and PA-7300 LC processors used LASI and GSC as system and I/O bus.

U2/UTurn: PA-RISC computers based on 32-bit and 64-bit processors with a Runway processor interface used a U2 or UTurn system design that attached GSC- and PCI-based I/O and memory via

adapters to the Runway bus.

Astro: Some PA-8500, PA-8600 and PA-8700 systems use a rope-based architecture with Astro as main system controller and Runway+ buses with I/O devices controlled by Elroy PCI bridges.

Stretch: Stretch was a 64-bit system design for midrange servers based on PA-8500 to 8700 processors, with a central system controller and links to processor and I/O controllers and PCI bridges. The main system bus is Itanium with converters for the PA-RISC processor Runway bus.

Cell: This was a crossbar chipset used in few HP 9000 Integrity servers and some Superdome models. The main design feature were individual system or processor "cells" that were interconnected by a CEC component and central crossbars.

zx1: The zx1 chipset was a HP Itanium chipset bus used in later HP 9000 and Integrity PA-RISC servers as well. It consists of two purpose-built main parts that connect the processor, memory and I/O to the Itanium system main buses: Pluto and Mercury.

2.4.1 Early designs

Early 32-bit PA-RISC systems, such as the 1980s TS-1, NS-1, NS-2 and PCX, used custom designs based on the SIU/SPI main bus interfaces and the SMB bus. The computing and I/O units consisted of a large number of individual chips to form the central chipset and used the CIO and HP-PB I/O buses. The first PA-RISC 1.0 processors used external support chips to attach the CPU to memory and I/O. This functionality was later integrated into single chips and then moved to the CPU altogether.

- **SIU** or **SPI** system interface unit attaches the CPU to the SMB system main bus
- *NS-1* Two cache controller units CCU0 and CCU1
- *NS-2* Two CCUs cache controller units ICCU and DCCU
- *PCX* Three CMUX cache multiplexers
- Physical address space of 29-bit to support up to 512 MB main memory
- System Main Bus SMB is the central bus, to which CPU, memory and I/O buses attach with 64-bit at 25-30MHz.
- Memory is attached to the SMB main bus
- Central Bus or Midbus CTB attaches the I/O via bus converters to SMB, 32-bit at maximum of 10 MHz
- CIO buses for I/O devices attach via adapters to CTB, 16-bit at 4 MHz, I/O expansion cards plug into CIO slots

Systems using these early designs, in various, slightly different variants:

- HP 9000 800 servers: 840, 825, 835, 850, 822, 832, 845, 855, 860, 842, 852, 865, 870.

2.4.2 ASP chipset

HP 9000 workstations and servers based on the 32-bit PA-7000 and PA-7100 processors use the ASP chipset together with the Viper memory controller. Being an integrated chipset, ASP includes separate chips to provide the I/O subsystem and contains several modules from third-party vendors. Some HP 9000 800 servers use a partial implementation of ASP.

- VSC interface to system main bus, 32-bit, to the Viper memory controller
- GSC interface to main I/O bus, also sometimes called "SGC"
- NCR 53C700 8-bit Narrow single-ended SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller, and Intel 82501AD Ethernet transceiver, media auto-selection
- EISA bridge based on the Intel 82350 chipset
- Domain keyboard controller
- WD 16C552 parallel and NS 16550A compatible serial
- Intel 8042 microprocessor
- 512 KB EPROM Boot ROM, 8 KB EEPROM for storing system configuration status etc.
- 25-33 MHz chipset clock frequency on a 160-pin QFP chip

There are two variants of ASP for workstations: Coral or "Cobra I/O subsystem" is the original ASP, while "Hardball" is the second version ASP2, an improved design with fast/wide SCSI and FDDI networking, used on the 735/755 workstations:

- NCR 53C720 16-bit Fast-Wide differential SCSI-2
- AMD Formac Plus Am79C830 FDDI controller
- Stereo/CD quality audio
- Two 32-bit device data buses, a variant of GSC bus: one attaches to LAN and FDDI, the other to two SCSI controllers, audio and other I/O devices
- ASP2 consists of two separate chips: Shortstop, main bus and memory interface, and Cutoff, the main address controller

Viper

Viper is the memory and I/O controller MIOC on systems with PA-7000 and PA-7100 processors. The chip is similar on both, and sometimes counted into the ASP I/O chipset. It handles all memory and I/O traffic between the processor and the rest of the system.

- Viper attaches with 32-bit multiplexed address/data bus PBus to the CPU
- Memory attaches directly to Viper, with multiplexed 64-bit ECC
- VSC system main bus attaches to Viper, 32-bit on PA-7000, 64-bit on PA-7100
- I/O attaches with bus adapters to VSC bus
- Viper is also called MIOC, PMI or PIC

- On SMP systems either each CPU has its own MIOC which share a SMB bus and memory, or two CPUs share one MIOC
- 9,5×9,5 mm^2 die, 185,000 FETs, 0.8µ, CMOS26B in 272-pin CPGA
- Newer/different Viper design: 0.8µ, CMOS26B in 408-pin PGA
- SBI system bus interface: two 100-pin QFP chips
- Low-cost version on the 705/710 workstations: two separate chips, each 7,0×7,0 mm^2 die, 1.0µ, two-layer metal CMOS34 in 160-pin QFP

Used in

- 705, 710, 715, 725, 720, 730, 750, 735, 755, 742i, 745i, 747i
- Nova servers (F, G, H, I-Class)
- 890, T500, T520
- Mitsubishi ME/R7200, ME/S7200, ME/R7300, ME/S7300, ME/R7500, ME/S7500
- Hitachi 3050RX 220, 230, 310S, 320, 330, 430, 440, 9000V V735/125, VT500

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2.4.3 LASI chipset

PA-7100LC and PA-7300LC systems use the highly integrated LASI chipset, which combines most functions and I/O on a single chip and an on-CPU MIOC memory controller.

LASI was primarily designed for cost-reduction while still providing most I/O functions. It was used as the main controller in most PA-7100LC and PA-7300LC systems, while later 64-bit PA-8x00 systems used LASI for complementary I/O functions. The primary cost reductions were achieved by integrating the major I/O subsystems into a single chip, like **LA**N SC**SI**. and some designed specifically for LASI. The LC CPUs integrate the external memory and I/O controller MIOC onto the processor with memory and cache directly attaching to it.

- GSC bus interface
- Integrated Intel i82C596CA 10 Mbit Ethernet controller
- Integrated NCR 53C710 Fast-Narrow SE SCSI-2 controller
- NS16550A compatible RS232, WD16C522 compatible parallel
- *Harmony* CD-quality 16-bit sound
- PS/2 style keyboard and mouse devices
- External 8-bit bus to connect flash EPROMs and a FDD controller
- Bus arbitration, Interrupt controller, Real-Time clock, PLL generator for the whole I/O subsystem
- 13.2×12.0 mm^2 die, 520,000 FETs, 0.8µ, CMOS26B in 240-pin MQUAD, 3W power at 40 MHz

A typical system design with one of the 32-bit LC "Low Cost" processors PA-7100LC and PA-7300LC wht GSC main system bus would look like this:

1. MIOC, main memory and I/O controller, directly integrated on the CPU
   - Execution units and internal caches attach on-chip to the MIOC
   - External cache and memory attach to MIOC
2. GSC, system main bus, attaches to MIOC and I/O controllers
   - Attaches via 32-bit
   - PA-7300LC systems use extended GSC+
3. I/O adapters attach to GSC
   - LASI chipset
   - Some video adapters directly attach to GSC
   - I/O slots extend GSC
   - Bus adapters, including EISA, VME and PCI, attach to GSC

Memory and I/O Controller (MIOC)

The *Memory and I/O Controller* in the PA-7100LC and PA-7300LC processor integrates DRAM/cache and I/O controller onto the processor die. It is similar on both CPUs, with the PA-7300LC MIOC having wider data paths to L2 cache and RAM and supporting the advanced GSC+ bus over the older GSC.

The integrated memory controller requires only buffers and DRAM modules to build up the complete memory subsystem. The PA-7300LC memory controller includes a Second Level Cache Controller SLC, which provides an optional L2 cache, ranging from 32 KB to 8 MB. It shares the data bus with the DRAM subsystem, so it has the same width and same optional SEDC error control.

- Execution units and internal caches attach on-chip to the MIOC
- External cache, L1 on PA-7100LC, L2 on PA-7300LC, attach to MIOC via 64-bit or 128-bit
- Memory attaches to MIOC via 64-bit, on PA-7100LCm or 128-bit, on PA-7300LC
- GSC, the system main bus, attaches to MIOC
- Support for 4, 16, 64 and 256 Mbit modules, both FPM and EDO DRAM at 3.3 or 5.0 V
- Up to 16 physical memory slots
- Support for a wide range of core frequencies

Wax

Wax is a secondary I/O controller complimentary to the LASI chipset. It implements various secondary I/O functions and acts as a I/O bus to GSC adapter for different external buses as EISA, HP-HIL and HP-IB. Most systems use it to complement LASI with other required I/O functions that were previously implented in diverse I/O ASICs. It is implemented in the same process and package as LASI.

- GSC bus interface with GSC**+** features
- EISA bus converter, interfaces to external EISA controller: TI TACT84500
- Serial interface — NS16550A compatible RS232
- HP-HIL interface, compatible to previously separate HP HIL chip used in older workstations
- HPIB interface for instrumentation devices, needs three external chips
- Interrupt control, Timers
- 0.8µCMOS26B packaged in 240-pin MQUAD

Used in

- 712, 715, 725, 743i, 745, 744, 748i
- A180, A180C
- B132L, B132L+, B160L, B180L+
- C100, C110, C132L, C160L, C160, C180, C200, C240, C360
- D-Class
- E25, E35, E45, E55
- J200, J210, J210XC, J280, J282, J2240
- K-Class
- RDI PrecisionBook 132, 160, 180

- R380, R390
- SAIC Galaxy 1100
- HP Agilent 16600A, 16700A, 16700B, 16702A and 16702B series logic analyzers

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2.4.4 U2 and UTurn chipset

PA-RISC computers based on 32-bit and 64-bit processors with a Runway processor interface used a U2 or UTurn system design and chipsets. U2 and UTurn are the I/O adapters and MMC/SMC the memory controllers that each attach other subsystems to the main Runway processor bus. Also called IOAs, UTurn and U2 attach the GSC main system bus with devices and I/O to the Runway to the processors. This setup allowed HP to use a standard frontend with UTurn in different system designs with different backends to support memory or I/O technologies.

U2 is the variant for PA-7200 systems while all later systems with PA-8000 and PA-8200 processors use the UTurn follow-on.

- Runway bus interface to CPU/memory bus, 64-bit wide, 120 MHz, 960 MB/s peak bandwidth
- U2: Two GSC+/HSC I/O buses, peak bandwidth between 128 MB/s to 160 MB/s each
- UTurn: Two GSC-2 I/O buses, peak bandwidth 256 MB/s each
- Support for various frequencies on both sides on Runway and GSC
- Address translation from 32-bit GSC to 40-bit Runway addresses
- Interface to processor dependent hardware PDH on IOA A
- Hardware cache coherent I/O
- Real-time clock
- U2 is a 432-pin PGA chip, chip numbers: 1MM6-0004

A typical system design and bus setup would look the following:

- Runway is the main processor and memory bus for 1-4 CPUs at 64-bit
- MMC is the main memory controller which attaches to Runway at 64-bit
  - Memory attaches to MMC via slave Memory Controllers SMC and Data Multiplexers, 128-bit 60 MHz data and 39-bit 60 MHz address buses
- U2/UTurn I/O adapters attach the system bus to the Runway processor bus at 64-bit
- GSC+, the main system bus, attach to the U2/UTurn IOAs at 32-bit
- I/O adapters and slots attach to GSC+
  - LASI chipset
  - Video adapters
  - I/O slots extend GSC
  - Bus adapters, including EISA, VME and PCI, attach to GSC+

MMC/SMC

Most systems with a PA-7200, PA-8000 or PA-8200 processor use a combination of the MMC and SMC memory controllers to attach the main system memory to the Runway processor bus. The I/O is controlled by the U2/UTurn I/O adapters on the same Runway bus.

- Master Memory Controller MMC attaches with 64-bit to the Runway processor bus and 128-bit to the memory, 960 MB/s data rate

- Up to eight Slave Memory Controllers SMCs attach to one MMC on its memory address bus. The SMCs carry the functionality to interface with specific types of DRAM.
- Data Multiplexers DMs attach the 128-bit 60 MHz data bus of the MMC to memory banks. Each two sets of memory connect with two 64-bit 30 MHz buses to the DMs.
- Physical address space of 36-bit for 32 GB main memory
- Memory address bus is shared between all SMCs of a MMC, 39-bit at 60 MHz
- Memory data bus attaches to the DMs and memory

Used in

- C100, C110C160, C180, C200, C240, C360
- D-Class
- J200, J210, J210XC, J280, J282, J2240
- K-Class

Dino/Cujo

Dino is the GSC to PCI bridge found in many older PCI PA-RISC workstations. The GSC and PCI buses do not need to be synchronized, simplifying the system design. Dino also implements a small set of I/O functions. Cujo is a Dino bridge for 64-bit PCI.

- GSC bus interface with GSC+ feature, >40 MHz
- PCI bus interface (PCI64 on Cujo), >33 MHz
- Two PS/2 interfaces, RS-232 port
- Mapping register with 8 MB resolution
- Integrated PCI arbitration
- Integrated interrupt register
- Supports both 3.3 V and 5.0 V PCI operation

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2.4.5 Astro chipset

Some PA-8500, PA-8600 and PA-8700 systems use a "rope"-based architecture with Astro as main system controller and IOMMU, and separate Runway+/Runway DDR buses with I/O devices controlled by Elroy PCI bridges.

- Runway+/Runway DDR is the main processor and memory bus: one to four CPUs attach to Runway with 64-bit, parity-protected.
- Astro is the main memory and I/O controller which attaches to Runway: memory attaches to Astro with a peak data rate of about 2.0 GB/s at 125 MHz, and up to eight I/O links (ropes) with each 250 MB/s attach to Astro.
- Elroy I/O adapters attach PCI bridges via the I/O ropes to Astro: One or two ropes per Elroy PCI bridge, then PCI slots or devices attach to Elroy bridges
- PCI buses attach to the multiple Elroy bridges, in 33 or 66 MHz, 32 or 64-bit variants. I/O devices, adapters and slots attach to PCI
- Astro supports 120/125 MHz SDRAMs for a maximum supported memory of 40 GB
- Pluto is the successor of Astro for Itanium-2 processors and buses; it works very similar.
- 16-entry fully associative I/O TLB
- 16-entry fully associative coherent I/O buffer cache

Elroy

Elroy is a PCI bus bridge that attaches one PCI bus to one or more I/O ropes. Elroy was often used with the Astro memory and I/O controller.

- Peak bandwidth of up to 500 MB/s
- Multiple Elroys can be used in a single system
- Support for *Turbo* and *Twin Turbo* slots — attached via one or two links respectively
- Support for PCI 2.1, 1X, 2X and 4X bus
- PCI data width of 32 or 64 bit
- PCI clock of 33 or 66 MHz

Used in

- A400 (rp2400, rp2430), rp2405, A500 (rp2450, rp2470)
- B1000, B2000, B2600
- C3000, C3600, C3700
- J5000, J5600, J6000, J6700, J7000, J7600
- L1000 (rp5400), L2000 (rp5450), L1500 (rp5430), L3000 (rp5470)
- Elroy: N4000 (rp7400), N4000 (rp7405, rp7410),

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   Astro External Reference Specification Memory Map
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2.4.6 Stretch system design

Stretch was a 64-bit HP PA-RISC system design for midrange servers based on PA-8500 to 8700 processors, a complicated setup with a central system controller and "links" to processor and I/O controllers and PCI bridges. The main system bus is an Itanium bus, with converters for the processors' Runway+/Runway DDR buses. There are four main components, and the following buses used:

- Prelude memory controller connects the main memory to two system buses.
- DEW Runway ports/converters convert the system buses into Runway buses for the PA-8500 and upwards CPUs — two CPUs share one DEW.
- IKE I/O controllers attach PCI bridges via I/O links to the system bus.
- Elroy PCI bridges convert the I/O channels from IKE I/O controllers into PCI buses

Prelude

Prelude is the memory controller of systems with the Stretch chipset and connects the up to 16 pairs of SDRAM memory via four memory buses to two system buses. The main buses are in fact Itanium/Merced buses in preparation of the HP shift from PA-RISC to Itanium. Prelude consists of three VLSI chips: one address controller and two data controllers; each data controller drives two multiplexed 64-bit memory buses:

- Two system buses, each 2.1 GB/s peak with 4.3 GB/s aggregate
- Up to four memory buses, each 2.1 GB/s peak with 8.6 GB/s aggregate to the memory
- Both memory and system buses are Itanium/Merced buses at 133 MHz DDR with 64-bit width, ECC-protected
- System main buses connect to the CPU bridges (DEW) and I/O controllers (IKE)

DEW

DEW is the Runway CPU bridge for systems based on the Stretch chipset. It attaches the Runway-based PA-8500, PA-8600 and PA-8700 CPUs to the Itanum-based system man buses. Each pair of two CPUs share one DEW port converter. Common configurations include one to four DEWs for up to eight processors.

- CPU side: Runway+/Runway DDR processor bus for up to two PA-8x00 processors with peak bandwidth of 2.1 GB/s
- System side: Itanium system bus at 133 MHz, with 2.1 GB/s peak

IKE

IKE is the I/O controller on systems with the Stretch chipset. The central memory controller provides one or two system buses, to which CPUs and I/O attach. Each system bus has one IKE I/O controller that connects to several slave I/O controllers (Elroy PCI bridges), which in turn provide PCI buses. The connection between IKE and each slave I/O controller is one or two 12-byte wide I/O links (I/O ropes). I/O channels can be combined into twin I/O channels for so-called "Twin-Turbo" PCI slots/buses.

- System side connects to system main bus, a Itanium bus at 133 MHz, with 2.1 GB/s peak
- I/O side attaches to up to twelve 12-byte wide 266 MB/s I/O links
- Each PCI slot has its own PCI controller and bus
- Elroy PCI bridges convert the I/O channels into PCI buses

Used in

- L1500 (rp5430), L3000 (rp5470)
- N4000 (rp7400)

References

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2.4.7 Cell chipset

Cell is a crossbar chipset used in HP 9000 PA-RISC Integrity servers and some Superdome mainframe computers. The Central Electronics Complex CEC interconnects individual system and processor "cells" via central crossbars. The cell boards were seated in the backplane of the system, which provided the cell-to-cell links and I/O functionality.

The CC Cell Controller is the central chipset at the core of each cell. It connects local processors and memory on cells to the SBA I/O links and the XBC crossbar. XBC is the crossbar ASIC that provides the main backplane function, each backplane supports up two four cell modules. Different backplanes can be tied together through links through the XBCs with a high-bandwidth, low/latency connection.

M2 are the main memory controllers and converters on each cell board. There are eight M2 controllers that attach in two banks to each CC. Requests and addresses are sent directly from the CC to memory, with the data returning through the M2s.

RIO is the master I/O controller, also called SBA. The central I/O part of the main chipset, with one SBA reserved for each cell/CC, located on the (I/O) backplane. Each SBA provides sixteen 12-bit links called ropes to which slave I/O controllers connect, the LBAs. These LBAs are Elroy PCI bridges that convert the links from the SBA into PCI buses.

Core I/O is a card set that provides standard I/O functions and plugs into PCI-64 or special slots to provide third-party I/O functions. Distinct cards were availaible: MP/SCSI card and LAN/SCSI, among others.

- Two dual-channel Symbios Logic 53C1010 Ultra160 SCSI controllers
- Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller
- Gigabit Ethernet networking
- Console, serial and management controllers
- Fast-Ethernet DEC 21142/43 for Management LAN
- Optional second Core I/O card for redundancy or partitioning

Several buses were used in Cell: Runway+ processor bus for up to four processors at 8.0 GB/s. Memory bus to the M2, for up to two memory "banks" with 4.0 GB/s peak The SBA I/O links to the off-cell SBA have 2.0 GB/s peak, the XBC link to the crossbar for cell-to-cell communication 8.0 GB/s peak.

Used in

- N4000 (rp7405, rp7410)
- Superdome

References

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- User Guide hp rp7405/7410 Servers (URL gone)

2.4.8 zx1 chipset

The zx1 chipset was a HP Itanium chipset bus used in later HP 9000 and Integrity PA-RISC servers as well. It consists of two purpose-built main parts that connect the processor, memory and I/O to the Itanium system main buses: Pluto and Mercury.

- Pluto zx1 memory and I/O controller (MIO) is the main chipset controller
  - Processor bus
  - Two independent memory buses
  - I/O channels (I/O ropes)

  Pluto also contains memory and cache controllers. Part of the memory subsystems are sometimes the zx1 SMEs scalable memory expanders that increase memory capacity and data rate through multplexing
- Mercury zx1 I/O adapters IOAs connect PCI-X/AGP slots and I/O devices to Pluto

The rest of the I/O chipset is made up of standard third-party, such as SCSI controllers, Ethernet.

Pluto

Many of the Itanium-based HP workstations and servers use the Pluto I/O and memory controller as part of the zx1 chipset. Pluto is based on the Astro IOMMU, extending it for Itanium-2 processors and bus interfaces, DDR memory and faster I/O links.

- Processor bus: Itanium-2 processor bus for up to four CPUs, maximum of 200 MHz bus with 128-bits for up to 6.4 GB/s data rate.
- Two memory buses with peak 8.0 GB/s at maximum clock of 266 MHz DDR.
- I/O system based on eight separate 500 MB/s I/O links for individual PCI, PCI-X or AGP bridges. Peak aggregate I/O bandwidth is 3.2 GB/s
- Support for DDR SDRAMs
- Maximum supported memory of 16 GB to 64 GB with SME memory extender
- 16-entry I/O TLB
- 16-entry coherent I/O cache

Mercury

Mercury is a PCI/AGP bridge for systems based on I/O ropes. It is part of the zx1 chipset used on Itanium systems (alled zx1 I/O adapter, and based on the Elroy PCI bridge, extending it for AGP devices and faster I/O ropes. Most systems use several Mercury chips to attach PCI/AGP buses to the multiple I/O ropes. Each Mercury attaches one PCI or AGP bus to up to four 500 MB/s I/O ropes.

Mercury is most often used together with the Pluto I/O and memory controller of the zx1 chipset.

- Attaches to one to four (bundled) I/O ropes
- Provides one PCI, PCI-X or AGP 2.0 bus
- Multiple Mercurys can be used in a single system

- Support for PCI 2.1, also some support for PCI 2.2
- Support for PCI-X
- Support for AGP 1X, 4X and 4X
- PCI data width of 32 or 64 bit
- PCI clock of 33 or 66 MHz
- PCI-X clock of up to 133 MHz
- Up to six PCI slots
- No support for 5 V PCI

Used in

- rp3410, rp3440, rp4410, rp4440, rp7420
- rx1600, rx1620, rx2600, rx2620, rx2660 rx3600, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640
- Superdome
- zx2000, zx6000

References

- zx1 mio (Memory and I/O) External Reference Specification Hewlett-Packard Company (March 2003, Revision 1.0)
- HP zx1 ioa ERS External Reference Specification Ropes to AGP/PCI/PCI-X Bridge (.pdf) Hewlett-Packard Company (April 2003, Revision 3.2)

2.5 PA-RISC Buses

2.5.1 Overview

Many different buses and bus systems were used in PA-RISC computers. Some were custom HP designs, especially the system main buses and early I/O buses such as VSC and GSC. For I/O devices HP used some custom designs as well but made use of industry buses such as EISA, PCI and others soon.

Table 2.9: Buses used in PA-RISC computers overview

Type	Frequencymax	Width	Data ratemax	Usage
GSC	40 MHz	32-bit	160 MB/s	System bus
HSC/GSC+	40 MHz	32-bit	160 MB/s	System bus, also: I/O
GSC-2	40 MHz?	32-bit	256 MB/s	System bus, also: I/O
VSC PA-7000	60 MHz	32-bit	240 MB/s	System bus
VSC PA-7100	60 MHz	64-bit	480 MB/s	System bus
SMB	30 MHz	64-bit	?	System bus
PBus	66 MHz?	64-bit	?	CPU
Runway	120 MHz	64-bit	960 MB/s	CPU
Runway+	125 MHz	64-bit	~2 GB/s	CPU
EISA	8.3 MHz	32-bit	33 MB/s	I/O bus
SGC	25 MHz?	32-bit	100 MB/s	I/O bus
HP-PB	8 MHz	32-bit	32 MB/s	I/O bus
PCI-32	66 MHz	32-bit	266 MB/s	I/O bus
PCI-64	66 MHz	64-bit	533 MB/s	I/O bus
PCI-X	133 MHz	64-bit	1066 MB/s	I/O bus

2.5.2 System buses

GSC

The General System Connect GSC bus is the primary system and I/O bus on most of second-generation 32-bit HP 9000 workstations. GSC connects most of the I/O devices to the central system bus and chipset, with some CPUs attaching directly to it like the PA-7100LC and PA-7300LC HSC is a variant of GSC.

GSC bus features

- 32-bit data path width
- Multiplexed address and data
- Transfer rates of up to 142-256 MB/s, depending on bus variant
- 5 V signalling voltage

Bus variants

1. Original GSC, GSC-1X, with maximum clock of 40 MHz and peak data rate of 160 MHz, used on most of the early GSC systems, mostly together with LASI as main I/O controller

2. GSC+/HSC, Extended GSC, with a maximum clock of 40 MHz and peak data rates of 160 MB/s, 132 MB/s with 33 MHz, 144 MB/s with 36 MHz
3. GSC-1.5X with additional extended write operations
4. GSC-2 or GSC-2X, with a peak data rate of 256 MB/s on 64-bit systems with the UTurn I/O bridge to Runway

Expansion cards variants

- EISA-like
  - Both GSC-1X and GSC-2X, also probably GSC-1.5X
  - 100-pin female EBBI card connector
- GIO
  - Limited to the 712 workstation
  - GSC-1X
  - 80-pin female EBBI card connector GIO formfactor
- HSC High-speed System Connect
  - On several server systems, for example D-Class and K-Class
  - Cards are all GSC+
  - 100-pin male pin and socket with groundplane
  - Identical to GSC-M cards except different bulkhead
- GSC-M "Mezzanine"
  - Found on PA-RISC VME computers, the 74x
  - GSC-1X
  - 100-pin male pin and socket with groundplane
  - Cards are very rare
  - Identical to HSC cards except different bulkhead

VSC

Viper System Connect VSC is the central system bus of computers with PA-7000 or PA-7100 processors. It connects the Viper central bus controller, also known as MIOC, PMI or PIC, to the memory and I/O buses. In multiprocessor configurations, each processor has its own Viper controller, which then in turn connects to a *shared* VSC bus with attachments to all Viper controllers, memory and I/O converters.

- 32-bit data path width on PA-7000 systems
- 64-bit data path width on PA-7100 systems
- 128-bit data path width possible, apparently only implemented on the T500 servers
- Synchronous pipelined bus

- ◈ Separate data and address buses
- ◈ Memory data blocks are transferred in 16, 32 or 64 Byte blocks
- ◈ Provides cache and TLB coherency on multi-processor configurations as a snoopy bus
- ◈ Various clock speeds were supported, as a ratio of the processor clock speed 2/3 was common
- ◈ Maximum data rate depends on clock speed and bus width, with a common configuration of 60 MHz and 64-bit: 480 MB/s
- ◈ Apparently 3.0V signalling voltage

System Main Bus (SMB)

In early 1980s PA-RISC 1.0 systems the NS-1, NS-2 and PCX processors attach to the System Main Bus SMB, via bus converters.

- ◈ 64-bit data width
- ◈ Clockspeed of maximum 25-30 MHz
- ◈ Central system bus between CPU/bus adapter, memory and I/O buses

The TS-1, the first PA-RISC processor used a simpler version of this setup and directly attached the CPU to the Central Bus CTB with 32-bit at 8 MHz. Here, all the CPU, memory and I/O devices directly connect to the CTB.

2.5.3 CPU buses

PBus

Systems with PA-7000 or PA-7100/PA-7150 processors use the PBus processor bus between the CPU and external memory controller Viper. These systems with the VSC main bus mostly use ASP chipsets for system I/O and devices. On multi-processor systems with a PA-7100 two attachment variants are possible — either shared memory controller on two processors or shared system bus with up to eight processors.

Bus features

- ◈ 32-bit multiplexed address/data bus
- ◈ Runs at fixed fractions of CPU clock, 1.0, .67 and .50 of processor speed
- ◈ Two multiprocessor strategies supported on the PA-7100

CPU attachment

1. **PBus** is the main processor and memory bus
   - ◈ CPU attaches to PBus with 32-bit, with ECC 40-bit
2. **Viper**, the main memory and I/O controller attaches to PBus
   - ◈ Memory attaches to MIOC via 64-bit, with ECC 72-bit
3. **VSC**, the system main bus, attaches to MIOC and various I/O controllers

- ◇ Attaches via 32-bit on PA-7000 or 64-bit on PA-7100 at MIOC

4. I/O adapters attach to VSC
   - ◇ Either ASP chipset for SGC or GSC bus systems, or HP-PB adapters for some servers

Multiprocessor attachment

1. Two-way SMP "Low Cost" : Two CPUs share a PBus and attach to the same MIOC. Memory attaches directly to MIOC, I/O attaches via VSC to MIOC.
2. Scalable MP: Each CPU has its own MIOC. All MIOCs in the system share a VSC bus, to which I/O and memory attach.

Runway

Runway is the system bus of newer 64-bit systems with PA-7200 and PA-8000 processors and up. It is a synchronous, split-transaction bus. PA-8500, PA-8600 and PA-8700 use an advanced version of Runway, Runway+/Runway DDR.

Bus features

- ◇ 64-bit multiplexed address/data
- ◇ 20 bus protocol signals
- ◇ Supports cache coherency
- ◇ Three frequency options of 1.0, 0.75 and 0.67 of CPU clock — 0.50 apparently was later added
- ◇ Parity protection on address/data and control signal
- ◇ Each attached device contains its own arbitrator logic
- ◇ Split transactions, up to six transactions can be pending at once
- ◇ Snooping cache coherency protocol
- ◇ 1-4 processors "glueless" multi-processing with no support chips needed
- ◇ 768 MB/s sustainable throughput, peak 960 MB/s at 120 MHz
- ◇ Runway+/Runway DDR: On PA-8500, PA-8600 and PA-8700, the bus operates in DDR *double data rate* mode, resulting in a peak bandwidth of about 2.0 GB/s Runway+ or Runway DDR with 125 MHz

Runway CPU attachments

The PA-7200, PA-8000 and PA-8200 processors with the Runway bus use split I/O and memory controllers — the U2/UTurn I/O Adapters IOAs and MMC/SMC memory controllers with each what can be called "frontends" and "backends" , with the former interfacing to the CPU and its processor bus and the latter attaching the frontend to customized bus attachments on their external side. This allowed HP to use the frontend parts of these chipsets with a variety of different system design which only required modified backend parts for new memory or I/O technologies.

1. **Runway** is the main processor and memory bus

- 1-4 CPUs attach to Runway with 64-bit, parity-protected
- SMP-capable

2. **MMC** is the main memory controller which attaches to Runway
   - Master Memory Controller MMC
   - Attaches to Runway with 64-bit, with for example of 120 MHz at a data rate of 960 MB/s peak
   - Memory attaches to MMC via slave Memory Controllers SMC and Data Multiplexers, 128-bit 60 MHz data ECC and 39-bit 60 MHz address buses
3. **U2/UTurn I/O adapters** attach the main I/O bus and system to the Runway processor bus
   - Attach to Runway with 64-bit
   - Two I/O adapters IOAs per U2/UTurn chip
   - Maximum data rate depends on Runway clock with 120 MHz and 64-bit: 960 MB/s
4. **GSC+**, the main system bus, attach to the U2/UTurn IOAs
   - Attaches via 32-bit at a fraction of Runway/IOA clock, mostly 40 MHz
   - PA-7300LC systems use the extended GSC version
5. I/O adapters and slots attach to GSC+
   - LASI chipset
   - Video adapters
   - I/O slots extend GSC
   - Bus adapters, including EISA, VME and PCI, attach to GSC+

Runway+/Runway DDR CPU attachments

The PA-8500, PA-8600, PA-8700 processors use an advanced version of the Runway system bus with increased data rate and utilized different I/O and memory controllers, with most using the Astro chipset IOMMU and few servers the sophisticated Stretch and Cell chipsets.

Described below is the common configuration with Astro chipset — for the Stretch/Cell bus attachments see their entries at the Chipset page.

1. **Runway+/Runway DDR** is the main processor and memory bus
   - 1-4 CPUs attach to Runway with 64-bit, parity-protected
   - SMP-capable
2. **Astro** is the main memory and I/O controller which attaches to Runway
   - Attaches to Runway+/Runway DDR with 64-bit at maximum of 125 MHz with in this case 2.0 GB/s peak data rate
   - Memory attaches to Astro with a peak data rate of about 2.0 GB/s at 125 MHz
   - Up to eight I/O links or ropes with each 250 MB/s attach to Astro
3. **Elroy I/O adapters** attach PCI bridges via the I/O ropes to Astro

- ◇ One or two ropes per Elroy PCI bridge
- ◇ PCI slots or devices attach to Elroy bridges

4. **PCI**, the main I/O buses, attach to the multiple Elroy bridges
   - ◇ 33 or 66 MHz, 32 or 64-bit
5. I/O devices, adapters and slots attach to PCI

2.5.4 I/O buses

EISA

Extended ISA or EISA is an device I/O and expansion bus that replaced the 1980s ISA bus in HP Unix workstations and servers. EISA buses are found in various early 32-bit workstations, either on-board or through a bus converter; this industry standard bus made it possible to use third-party, generic expansion cards such as network interfaces and SCSI controllers.

- ◇ 32-bit data path width
- ◇ 33 MB/s maximum data rate
- ◇ 8.33 MHz maximum frequency
- ◇ 5 V signalling voltage
- ◇ EISA slots also accept 8/16-bit ISA cards, downwards compatible
- ◇ 200-pin edge male card connector
- ◇ Bulkhead is left of the card

SGC

System Graphics Connect SGC is the main system bus of earlier 32-bit "series 700" workstations. The I/O controller, CPU/memory controller and expansion cards attach to the GSC bus in these systems. Expansion cards are available in two different form factors: "EISA" and "DIO" .

- ◇ 32-bit data path width
- ◇ 100 MB/s maximum data rate
- ◇ 5 V signalling voltage
- ◇ 176-pin female pin&socket card connector in the DIO-II formfactor
- ◇ 160-pin male EBBI card connector EISA formfactor

HP-PB

The HP-Precision Bus HP-PB, sometimes HP/PB, is the I/O bus in many older 32-bit HP servers. Two form factors/sizes of HP-PB expansion cards were sold: single and double.

- ◇ 32-bit data path width
- ◇ 32 MB/s maximum data rate

- 8 MHz maximum frequency
- 5 V signalling voltage
- 96-pin female pin+socket card connector

PCI

With PCI HP changed its HP 9000 workstation and server design to an industry standard expansion and device bus. This allowed for using more off-the-shelf I/O chips and cards. Some of HP's PCI expansion cards for HP 9000 computers are actually relabeled third-party products or OEM designs with a PA-RISC compatible firmware and HP-UX driver.

Proper HP-UX drivers are the limiting factor for generic third-party PCI expansion cards in PA-RISC systems. In most cases drivers are only available for the HP-branded products. Open source operating systems as Linux or OpenBSD support many more devices in their PA-RISC ports, since many drivers were taken over from other architectures.

Table 2.10: PCI buses used in PA-RISC computers overview

PCI	Clock	Width	Data ratemax	Signalling
PCI-32/33	33 MHz	32-bit	133 MB/s	3.3 V/5 V
PCI-32/66	66 MHz	32-bit	266 MB/s	3.3 V
PCI-64/33	33 MHz	64-bit	266 MB/s	3.3 V/5 V
PCI-64/66	66 MHz	64-bit	533 MB/s	3.3 V
PCI-X	66 MHz	64-bit	533 MB/s	?
PCI-X	100 MHz	64-bit	800 MB/s	3.3 V
PCI-X	133 MHz	64-bit	1066 MB/s	?

2.5.5 References

- A High-Performance, Low-Cost Multiprocessor Bus for Workstations and Midrange Servers William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)
- An I/O System on a Chip Thomas V. Spencer et al (April 1995, Hewlett-Packard Journal)
- HP-UX Workstation HCL (Hardware Compatibility List) PA-RISC (pp. 188-189, 191, 198) Hewlett-Packard Company (July 1998, 14th ed.)
- Corporate Business Servers: An Alternative to Mainframes for Business Computing (.pdf) Thomas B. Alexander et al (June 1994: Hewlett-Packard Journal)

2.6 PA-RISC Graphics Adapters

2.6.1 Overview

All HP 32-bit and many of the earlier 64-bit PA-RISC computers used HP-designed video adapters, based on a variety of buses (GSC, SGC, etc.), chipsets and form factors. Only with the later PCI-based adapters HP switched to using customized versions of mainstream graphics adapters from the Intel/i386 world. The following sections describe most of the older, HP-proprietary designs.

2.6.2 CRX

CRX graphics adapters were available in various different configurations for both the GSG and GSC bus in their different formfactors. All of these adapters were officially only supported in HP-UX up to 10.20, some may still work with 11.00.

The CRX cards output a fixed resolution of **1280×1024**. cards with SGC bus in the DIO-II formfactor use either one (grayscale), three (RGB) or four (RGB and sync) BNC connectors, while cards for SGC and GSC in the EISA formfactor and the mainboard-integrated CRX adapters use HD15 VGA connectors.

Table 2.11: HP CRX graphics adapters

Device	Color max	Double-buffering	3D accel	Bus/Formfactor Part-number
GRX	8-bit grayscale	software	-	SGC (DIO-II): A1924A
CRX	8-bit	hardware	-	SGC (DIO-II): A1659A
Stinger (CRX)	8-bit	software	-	SGC (integrated)
Artist (CRX)	8-bit	hardware	-	GSC (integrated)
CRX-24	24-bit	hardware software	-	SGC (DIO-II FF): A1439A SGC (EISA FF): A2673A
CRX-24Z	24-bit	-	yes	SGC (DIO-II FF): A1454A SGC (EISA FF): A2674A
CRX-48Z	24-bit	hardware software	yes	SGC (DIO-II FF) + ext.: A2091A SGC (EISA FF) + ext.: A2675A GSC (EISA FF) + ext.: A4073A/B + A4074A

Notes

1. The *Stinger* CRX adapter, integrated into some of the older ASP-based workstations (older 715, 725), supports four different resolution/refresh-rate combinations, which can be changed via a DIP switch on the back of the machine or in the PDC.
2. The *Artist* graphics adapter, as found on many LASI-based workstations, is technically identical to the CRX devices but supports much more resolutions and refresh rates, which can be configured in the boot ROM.
3. The **Z**-suffix denotes a CRX board with an optional 3D-acceleration board, containing a hardware 24-bit Z-buffer. These combined adapters (*e.g.*, CRX-24Z) support the same visuals as stand-alone versions (e.g. CRX-24) but always provide the 3D acceleration. The hardware acceleration can only be used in conjunction with the Starbase, PHIGS, PowerShade or PEX APIs.
4. CRX-48Z adapters are GSC or SGC interface cards with a separate external processing box, which provides the RGB output connectors.

2.6.3 HCRX

The HCRX are the successors to the CRX graphics adapters and were shipped in systems with the GSC bus, either integrated into the mainboard or as a separate expansion board. They output a fixed resolution of **1280×1024** and use a HD15 VGA connector.

Table 2.12: HP HCRX graphics adapters

Device	Color max	Double-buffering	3D accel	Bus/Formfactor Part-number
HCRX-8	8-bit	hardware software	-	GSC (EISA FF): A4070A/A4070B GSC (GSC-M FF): A4315A
HCRX-8Z	8-bit	%	yes	GSC (EISA FF): A4079A/A4079B
HCRX-24	24-bit	hardware software	-	GSC (EISA FF): A4071A/A4071B GSC (GSC-M FF): A4316A
HCRX-24Z	24-bit	%	yes	GSC (EISA FF): A4179A

Notes

1. The **Z**-suffix denotes a HCRX-board with an optional 3D-acceleration board, containing a hardware 24-bit Z-buffer. These combined adapters (*e.g.,* HCRX-24Z) support the same visuals as stand-alone versions (e.g. HCRX-24) but always provide the 3D acceleration. The hardware acceleration can only be used in conjunction with the Starbase, PHIGS, PowerShade or PEX APIs.

2.6.4 Visualize

The HP Visualize line of graphics adapters were used in a large number of PA-RISC workstations integrated onto the mainboard and in expansion cards of various types. All cards provide 2D hardware acceleration, used by HP's X11 server on HP-UX. The 3D hardware acceleration is available in conjunction with either of the Starbase, PHIGS, PowerShade or PEX APIs.

The Visualize cards use either a HD15 VGA or EVC connector.

Table 2.13: HP Visualize graphics adapters

Device	Resolution max	Color max	Double-buffering	3D accel	Bus/Formfactor Part-number
Visualize-EG (base)	1280×1024	8-bit	software	-	GSC (EISA FF): A4450A GSC (HSC FF): A3519A PCI: A4977A PMC (PCI mezzanine): A4979A
Visualize-EG (dual)	1280×1024	8-bit	software	-	GSC (EISA FF): A4451A
Visualize-EG (ext. mem)	1600×1200	8-bit	software hardware	-	GSC (EISA-FF): + A4452A
Visualize-8	1280×1024	8-bit	hardware	yes	GSC (EISA FF): A4441A
Visualize-24	1280×1024	24-bit	hardware software	yes	GSC (EISA FF): A4442A
Visualize-48	1280×1024	24-bit	hardware software	yes	GSC (EISA FF): A4244A
Visualize-48XP	1280×1024	24-bit	hardware software	yes	GSC (2-slot EISA FF): A4246A GSC (HSC FF): A4455A

2.6.5 Visualize-FX

The HP Visualize-FX graphics adapters were a more or less complete redesign in contrast to their Visualize predecessors. The architecture of the graphics processors is PA-RISC based, the higher-end models in fact include more than four PA-RISC CPUs to process the graphics. The **FX**s were the first HP cards to support the OpenGL X-Window Extension (GLX), in addition to the legacy 3D APIs (Starbase, PEX, PHIGS). These adapters were only available as PCI bus cards, with some using two slots.

The EVC connector present on some cards needs an adapter cable to connect to a HD15 VGA monitor. These cards support a maximum resolution of **1600×1200** or **1280×1024** on older monitors. Both Sync-on-Green and Digital-Sync output signals are supported.

Table 2.14: HP Visualize-FX graphics adapters

Device	**Color max**	**Double-buffering**	**3D accel**	**Output**	**Bus/Formfactor Part-number**
Visualize-FXE	24-bit	hardware software	yes	VGA	PCI 32-bit 66 MHz: A4982A, A4982B
Visualize-FX2	24-bit	hardware software	yes	EVC	PCI 64-bit 66 MHz: A4552A
Visualize-FX4/FX6	24-bit	hardware software	yes	EVC	PCI 64-bit 66 MHz: A4553A (FX4) PCI 64-bit 66 MHz: A4554A (FX6)
Visualize-FX5/FX10	24-bit	hardware software	yes	VGA, DVI-D, stereo	PCI 64-bit 66 MHz: A1264A (FX5) PCI 64-bit 66 MHz: A1264B (FX5pro) PCI 64-bit 66 MHz: A1298A (FX10) PCI 64-bit 66 MHz: A1298B (FX10pro)

Notes

1. Two different FXE models with different memory subsystems were shipped:
   - ◇ A4982A: 18 MB SGRAM, (3.5 MB max for textures)
   - ◇ A4982B: 24 MB SDRAM, (9.5 MB max for textures)

   The **A**-version is slightly faster due to the use of SGRAM.
2. The FX4 and FX6 cards support an optional 16 MB hardware texture memory module.
3. The FX5/10**pro** models integrate the raster and texture-processor onto a single chip, resulting in a better performance than the standard FX5/10 models.
   The onboard RAM is used as unified buffer, Z-buffer and texture storage:
   - ◇ FX5[pro]: 64 MB (48 MB max. for textures)
   - ◇ FX10[pro]: 128 MB (110 MB max. for textures)

2.6.6 FireGL-UX

The FireGL-UX high-end graphics adapter was based on ATI's FireGL2 board, often used in Intel i386 PCs. It provides full OpenGL hardware acceleration under HP's X server and is binary compatible with the Visualize FX10pro adapter.

Details:

- ◇ IBM GT1000 geometry engine
- ◇ IBM RC1000 raster engine
- ◇ 128 MB DDR SDRAM of unified frame buffer, Z-buffer and texture storage
- ◇ Digital DVI and 3-pin stereo output

- 64-bit, 66 MHz PCI card

It is about twice as fast as the Visualize FX10pro.

Supported resolutions and refresh rates:

Table 2.15: HP FireGL-UX graphics adapter supported resolutions

Resolution	Refresh rate	Color depth
640×480	100Hz	24-bit
800×600	100Hz	24-bit
1024×768	100Hz	24-bit
1152×864	100Hz	24-bit
1280×960	100Hz	24-bit
1280×1024	100Hz	24-bit
1600×1000	85Hz	24-bit
1600×1024	85Hz	24-bit
1600×1200	85Hz	24-bit
1792×1344	60Hz	24-bit
1920×1200	76Hz	24-bit

2.6.7 References

- **Graphics Administration Guide for HP-UX 10.20** Hewlett-Packard (n.d.)
- **Graphics Administration Guide for HP-UX 11.x** Hewlett-Packard (2006: B2355-IE003, Edition E0206)

2.7 PA-RISC SCSI

2.7.1 SCSI variants

HP 9000 workstations and servers mostly used industry-standard SCSI storage devices and controllers. Many different variants of SCSI were used in the various HP 9000 and PA-RISC families. The table lists some of the variants of SCSI found in PA-RISC computers.

Table 2.16: SCSI buses in PA-RISC computers

SCSI	Clock	Width	Data rate (max)	Devices (max)	Signals	Length (max)	Connector
Narrow SCSI	5 MHz	8-bit	5 MB/s	7	SE	6m	50-pin
Fast-Narrow SCSI	10 MHz	8-bit	10 MB/s	7	SE HVD	3m 25m	50-pin
Fast-Wide SCSI	10 MHz	16-bit	20 MB/s	15	SE HVD	3m 25m	68-pin
Ultra-Narrow SCSI	20 MHz	8-bit	20 MB/s	7	SE LVD HVD	1.5m 12m 25m	50-pin
Ultra-Wide SCSI	20 MHz	16-bit	40 MB/s	15	SE LVD HVD	1.5m 12m 25m	68-pin
Ultra2-Wide SCSI	40 MHz	16-bit	80 MB/s	15	LVD	12m	68-pin
Ultra160 SCSI	40 MHz	16-bit	160 MB/s	15	LVD	12m	68-pin
Ultra320 SCSI	80 MHz	16-bit	320 MB/s	15	LVD	12m	68-pin

2.7.2 SCSI chipsets

HP 9000 workstations and servers from HP used several common SCSI controllers for their drives and storage. These chips were sometimes integrated into the mainboard or available on plug-in cards.

Table 2.17: SCSI chipsets in PA-RISC computers

Chipset	Speed	Width	Data rate	Bus
53C700		Narrow	5 MB/s	GSC
53C710	Fast	Narrow	10 MB/s	GSC
53C720	Fast	Wide	20 MB/s	GSC
53C875	Ultra	Wide	40 MB/s	PCI
53C896	Ultra2	Wide	80 MB/s	PCI

2.7.3 SCSI adapters

SCSI adapters for the various expansion buses found in PA-RISC systems.

Table 2.18: SCSI expansion cards

Part	Bus	SCSI type	Signals	Boot	HP-UX
A2679A	EISA	Fast-Narrow	SE	no	9.0-11i/32-bit
25525A	EISA	Fast-Narrow	HVD		8.05-10.20
25525B	EISA	Fast-Narrow	HVD		8.05-11.0/32-bit

A2874-66005	GSC EISA FF	Fast-Wide	HVD	yes	9.05/11.0
A2969A	HSC	Fast-Wide	HVD	yes	10.01-11i
A3644A[2]	HSC	Fast-Wide	HVD		10.20-11i
A4107A	GSC EISA FF	Fast-Wide	HVD		9.05-11i/32-bit
A4268A	GSC-M	Fast-Wide	HVD	yes	9.05-11.0/32-bit
27251A	HP-PB				
28655A	HP-PB	Fast-Narrow	SE	yes	10.01-11i
28696A	HP-PB	Fast-Wide	HVD	yes	10.01-11i
A4800A	PCI	Fast-Wide	HVD	yes	10.2-11i
A4974A	PCI	Ultra-Wide	SE	yes	10.20-11.0
A4976A	PCI	Fast-Wide	HVD	yes	10.20-11.0
A4999A	PCI	Ultra2-Wide	LVD	yes	10.20-11.0
A5159A	PCI	Fast-Wide	HVD	yes	10.20-11i

Chapter 3

PA-RISC Computer Systems

3.1 Overview

Many different PA-RISC computers were developed by HP between the 1980s and 2000s. The popular HP 9000 family of Unix systems included many different types of PA-RISC servers, workstations and mainframes. HP later extended the PA-RISC range with HP Visualize workstations and Integrity **rp** and **rx** servers, where PA-RISC and the successor Itanium architecture slowly converged.

PA-RISC computers almost exclusively used custom HP PA-RISC designs for processors, chipsets and hardware from that time.

3.1.1 HP 9000 700 workstations

PA-RISC workstations were sold in many different formats, from rather small *712*, *715* and B-Class desktop to the heavy and powerful *735/755* and C-Class workstations.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
705	PA-7000 35 MHz	96 KB	128 MB	ASP	None	HP-UX, Linux, OpenBSD
710	PA-7000 50 MHz	96 KB	128 MB	ASP	None	HP-UX, Linux, OpenBSD
712/60	PA-7100LC 60 MHz	64 KB	128 MB	LASI	GIO, TSIO	HP-UX, Linux, NetBSD, NeXT, OpenBSD
712/80	PA-7100LC 80 MHz	256 KB	128 MB	LASI	GIO, TSIO	HP-UX, Linux, NetBSD, NeXT, OpenBSD
712/100	PA-7100LC 100 MHz	256 KB	192 MB	LASI	GIO, TSIO	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/33	PA-7100 33 MHz	128 KB	192 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/50	PA-7100 50 MHz	128 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/64	PA-7100LC 64 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/75	PA-7100 *75* MHz	512 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/80	PA-7100LC 80 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
715/100XC	PA-7100LC 100 MHz	1 MB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
720	PA-7000 50 MHz	384 KB	272? MB	ASP	EISA, SGC	HP-UX, Linux, OpenBSD
725/50	PA-7100 50 MHz	128 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
725/75	PA-7100 *75* MHz	512 KB	256 MB	ASP	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
725/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
730	PA-7000 66 MHz	384 KB	272 MB	ASP	EISA, SGC	HP-UX, Linux, OpenBSD
735/99	PA-7100 99 MHz	512 KB	400 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
735/125	PA-7150 125 MHz	512 KB	400 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD

750	PA-7000 66 MHz	512 KB	768 MB	ASP	EISA, SGC	HP-UX, Linux, OpenBSD
755/99	PA-7100 99 MHz	512 KB	768 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD
755/125	PA-7150 125 MHz	512 KB	768 MB	ASP2	EISA, SGC	HP-UX, Linux, NetBSD, NeXT, OpenBSD

3.1.2 Visualize workstations

PA-RISC workstations with lettered model names sold under the Visualize brand during the 1990s.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
B132L	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B132L+	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B160L	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B180L+	PA-7300LC 180 MHz	128 KB L1 (1 MB L2)	1.5 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
B1000	PA-8500 300 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
B2000	PA-8500 400 MHz	1.5 MB	4 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
B2600	PA-8600 500 MHz	1.5 MB	4 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C100	PA-7200 100 MHz	512 KB	1 GB	U2	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C110	PA-7200 120 MHz	512 KB	1 GB	U2	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C132L	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	2 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C160L	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	2 GB	LASI	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C160	PA-8000 160 MHz	1 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C180	PA-8000 180 MHz	2 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C200	PA-8200 200 MHz	1.5 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C240	PA-8200 236 MHz	4 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C360	PA-8500 367 MHz	1.5 MB	3 GB	UTurn	GSC, PCI, EISA	HP-UX, Linux, NetBSD, OpenBSD
C3000	PA-8500 400 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C3600	PA-8600 552 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C3650	PA-8700 625 MHz	2.25 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C3700	PA-8700 750 MHz	2.25 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
C3750	PA-8700+ 875 MHz	2.25 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD

C8000	2 PA-8800/ PA-8900 900 MHz/ 1.0 GHz/ 1.1 GHz	3 MB L1 32 MB L2/ 64 MB L2	32 GB	zx1	PCI-X, PCI, AGP	HP-UX, Linux
J200	1-2 PA-7200 100 MHz	512 KB	2 GB	U2	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J210	1-2 PA-7200 120 MHz	512 KB	2 GB	U2	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J210XC	1-2 PA-7200 120 MHz	2 MB	2 GB	U2	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J280	PA-8000 180 MHz	2 MB	2 GB	UTurn	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J282	1-2 PA-8000 180 MHz	2 MB	2 GB	UTurn	GSC, EISA	HP-UX, Linux, NetBSD, OpenBSD
J2240	1-2 PA-8200 236 MHz	4 MB	4 GB	UTurn	PCI, EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
J5000	1-2 PA-8500 440 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J5600	1-2 PA-8600 552 MHz	1.5 MB	8 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J6000	1-2 PA-8600 552 MHz	1.5 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J6700	1-2 PA-8700 750 MHz	2.25 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J6750	1-2 PA-8700+ 875 MHz	2.25 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J7000	1-4 PA-8500 440 MHz	1.5 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD
J7600	1-4 PA-8600 552 MHz	1.5 MB	16 GB	Astro	PCI	HP-UX, Linux, NetBSD, OpenBSD

3.1.3 Portable PA-RISC workstations

Three portable PA-RISC workstations were produced for mobile measurement and control by third-party vendors in the 1990s. The RDI and SAIC designs were based on modified HP 9000/712 and C132L workstation designs from HP and are rather rare.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
RDI PrecisionBook 132	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	512 MB	LASI	Cardbus	HP-UX, Linux, NetBSD, OpenBSD
RDI PrecisionBook 160	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	512 MB	LASI	Cardbus	HP-UX, Linux, NetBSD, OpenBSD
RDI PrecisionBook 180	PA-7300LC 180 MHz	128 KB L1 (1 MB L2)	512 MB	LASI	Cardbus	HP-UX, Linux, NetBSD, OpenBSD
SAIC Galaxy 1100	PA-7100LC 60 MHz	64 KB	128 MB	LASI	PCMCIA	HP-UX, Linux, NetBSD, OpenBSD
SAIC Galaxy 1100	PA-7100LC 80 MHz	256 KB	128 MB	LASI	PCMCIA	HP-UX, Linux, NetBSD, OpenBSD
Hitachi 3050RX/100C	Hitachi PA/50L	12 KB	80 MB	Other		HI-UX/WE2 (Hitachi)

HP 9000 800 servers

The HP 9000/800 were the original 32-bit PA-RISC servers with distinct architecture and heavy cases. The HP 9000/500 series were the original "HP 9000" computers and the predecessor to PA-RISC.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
520 (9020)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX, HP BASIC
530 (9030)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX, HP BASIC
540 (9040)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX, HP BASIC
550 (9050)	1-3 FOCUS 18 MHz	16 KB	10 MB	IOP/MPB	HP-IB, GP-IO, CIO	HP-UX, HP BASIC
635SV	NS-1 30 MHz	128 KB	96/112 MB	SIU	CIO	HP-UX, HPBSD,Mach 3/UX, Chorus
645SV	NS-2 27.5 MHz	256 KB	96/112 MB	SIU	CIO	HP-UX
808	PCX	32 KB	32 MB	SPI	HP-PB	HP-UX
815	PCX	32 KB	56 MB	SPI	HP-PB	HP-UX
822	NS-2 25 MHz	32 KB	128 MB	SIU	HP-PB	HP-UX
825	NS-1 25 MHz	16 KB	96/112 MB	SIU	CIO	HP-UX
832	NS-2 30 MHz	128 KB	128 MB	SIU	HP-PB	HP-UX
834 835	NS-1 30 MHz	128 KB	96/112 MB	SIU	CIO	HP-UX, HPBSD,Mach 3/UX, Chorus
840	TS-1 8 MHz	128 KB	96/112 MB	CTB	CIO	HP-UX
842	PCX 32 MHz	1 MB	? MB	SPI	HP-PB	HP-UX
845	NS-2 27.5 MHz	256 KB	96/112 MB	SIU	CIO	HP-UX
850	NS-1 27.5 MHz	128 KB	256 MB	SIU	CIO	HP-UX
852	PCX 50 MHz	1 MB	? MB	SPI	HP-PB	HP-UX
855	NS-2 27.5 MHz	256 KB	256 MB	SIU	CIO	HP-UX
860	NS-2 27.5 MHz	1 MB	256 MB	SIU	CIO	HP-UX
865	PCX 50 MHz	768 KB	512 MB	SPI	CIO	HP-UX
E25	PA-7100LC 48 MHz	64 KB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
E35	PA-7100LC 64 MHz	256 KB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
E45	PA-7100LC 80 MHz	256 KB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
E55	PA-7100LC 96 MHz	1 MB	512 MB	LASI	HP-PB	HP-UX, Linux, NetBSD
F10	PA-7000 32 MHz	96 KB	768 MB	Viper	HP-PB	HP-UX

F20	PA-7000 48 MHz	128 KB	768 MB	Viper	HP-PB	HP-UX
F30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G40	PA-7100 64 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G50	PA-7100 96 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
G60	PA-7100 96 MHz	2 MB	768 MB	Viper	HP-PB	HP-UX
G70	1-2 PA-7100 96 MHz	4 MB	768 MB	Viper	HP-PB	HP-UX
H20	PA-7000 48 MHz	128 KB	768 MB	Viper	HP-PB	HP-UX
H30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
H40	PA-7100 64 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
H50	PA-7100 96 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
H60	PA-7100 96 MHz	2 MB	768 MB	Viper	HP-PB	HP-UX
H70	1-2 PA-7100 96 MHz	4 MB	768 MB	Viper	HP-PB	HP-UX
I30	PA-7000 48 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
I40	PA-7100 64 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
I50	PA-7100 96 MHz	512 KB	768 MB	Viper	HP-PB	HP-UX
I60	PA-7100 96 MHz	2 MB	768 MB	Viper	HP-PB	HP-UX
I70	1-2 PA-7100 96 MHz	4 MB	768 MB	Viper	HP-PB	HP-UX

3.1.4 Lettered servers (HP 9000 800)

The "lettered" servers included 32 and 64-bit designs from the 700 and 800 series, from smaller towers in D-Class/E-Class to to deskside or cabinet systems in the K-Class.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
A180	PA-7300LC 180 MHz	128 KB	2 GB	LASI	GSC, PCI	HP-UX, Linux, NetBSD, OpenBSD
A180C	PA-7300LC 180 MHz	128 KB L1 1 MB L2	2 GB	LASI	GSC, PCI	HP-UX, Linux, NetBSD, OpenBSD
A400	PA-8x00	depends	2 GB	Astro	PCI	HP-UX, Linux
A500	1-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
D200	PA-7100LC 75 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD
D210	PA-7100LC 100 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD

D220	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D230	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D250	1-2 PA-7200 100 MHz	512 KB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D260	PA-7200 120 MHz	2 MB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D270	1-2 PA-8000 160 MHz	1 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D280	1-2 PA-8000 180 MHz	2 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D300	PA-7100LC 75 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD
D310	PA-7100LC 100 MHz	256 KB	512 MB	LASI	EISA, GSC	HP-UX, Linux, NetBSD
D320	PA-7300LC 132 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D330	PA-7300LC 160 MHz	128 KB L1 (1 MB L2)	1 GB	LASI	EISA, GSC	HP-UX, Linux, NetBSD, OpenBSD
D350	1-2 PA-7200 100 MHz	512 KB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D360	2 PA-7200 120 MHz	2 MB	1.5 GB	U2	EISA, GSC	HP-UX, Linux
D370	1-2 PA-8000 160 MHz	1 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D380	1-2 PA-8000 180 MHz	2 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
D390	1-2 PA-8200 240 MHz	4 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
K100	PA-7200 100 MHz	512 KB	512 MB	U2	HSC, HP-PB	HP-UX, Linux, NetBSD, OpenBSD
K200	1-4 PA-7200 100 MHz	512 KB	4 GB	U2	HSC, HP-PB	HP-UX, Linux, NetBSD, OpenBSD
K210	1-4 PA-7200 120 MHz	512 KB	4 GB	U2	HSC, HP-PB	HP-UX, Linux, NetBSD, OpenBSD
K220	1-4 PA-7200 120 MHz	2 MB	4 GB	U2	HSC, HP-PB	HP-UX, Linux, NetBSD, OpenBSD
K250	1-4 PA-8000 160 MHz	2 MB	4 GB	UTurn	HSC, HP-PB	HP-UX, Linux
K260	1-4 PA-8000 180 MHz	2 MB	4 GB	UTurn	HSC, HP-PB	HP-UX, Linux
K370	1-6 PA-8200 200 MHz	4 MB	4 GB	UTurn	HSC, HP-PB	HP-UX, Linux
K380	1-6 PA-8200 240 MHz	4 MB	4 GB	UTurn	HSC, HP-PB	HP-UX, Linux
K400	1-4 PA-7200 100 MHz	512 KB	2 GB	U2	HSC, HP-PB	HP-UX, Linux, NetBSD, OpenBSD
K410	1-4 PA-7200 120 MHz	512 KB	2 GB	U2	HSC, HP-PB	HP-UX, Linux, NetBSD, OpenBSD
K420	1-4 PA-7200 120 MHz	2 MB	8 GB	U2	HSC, HP-PB	HP-UX, Linux, NetBSD, OpenBSD
K450	1-4 PA-8000 160 MHz	2 MB	8 GB	UTurn	HSC, HP-PB	HP-UX, Linux

K460	1-4 PA-8000 180 MHz	2 MB	8 GB	UTurn	HSC, HP-PB	HP-UX, Linux
K570	1-6 PA-8200 200 MHz	4 MB	8 GB	UTurn	HSC, HP-PB	HP-UX, Linux
K580	1-6 PA-8200 240 MHz	4 MB	8 GB	UTurn	HSC, HP-PB	HP-UX, Linux
L1000	1-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
L1500	1-2 PA-8x00	depends	8 GB	Stretch	PCI	HP-UX
L2000	1-4 PA-8x00	depends	16 GB	Astro	PCI	HP-UX, Linux
L3000	1-4 PA-8x00	depends	16 GB	Stretch	PCI	HP-UX, Linux
N4000	1-8 PA-8x00	depends	32 GB	Stretch	PCI	HP-UX, Linux
N4000	2-8 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
R380	1-2 PA-8000 180 MHz	2 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux
R390	1-2 PA-8200 240 MHz	4 MB	3 GB	UTurn	EISA, GSC	HP-UX, Linux

3.1.5 Integrity (rp) servers

PA-RISC servers were called *rp* series around the turn of the century, almost all 64-bit rack systems.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
rp2400 rp2430 rp2405	PA-8x00	depends	2 GB	Astro	PCI	HP-UX, Linux
rp2450 rp2470 rp2405	1-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
rp3410	PA-8800 800 MHz	3 MB L1 32 MB L2	6 GB	zx1	PCI-X	HP-UX, Linux
rp3440	1-2 PA-8800 PA-8900 800 MHz-1.0 GHz	3 MB L1 32 MB L2 64 MB L2	32 GB	zx1	PCI-X	HP-UX, Linux
rp4410	1-2 PA-8800 PA-8900 800 MHz-1.0 GHz	3 MB L1 32 MB L2 64 MB L2	128 GB	zx1	PCI-X	HP-UX
rp4440	1-4 PA-8800 PA-8900 800 MHz-1.0 GHz	3 MB L1 32 MB L2 64 MB L2	128 GB	zx1	PCI-X	HP-UX
rp5400	1-2 PA-8x00	depends	8 GB	Astro	PCI	HP-UX, Linux
rp5430	1-2 PA-8x00	depends	8 GB	Stretch	PCI	HP-UX
rp5450	1-4 PA-8x00	depends	16 GB	Astro	PCI	HP-UX, Linux
rp5470	1-4 PA-8x00	depends	16 GB	Stretch	PCI	HP-UX, Linux
rp7400	1-8 PA-8x00	depends	32 GB	Stretch	PCI	HP-UX, Linux
rp7405	2-8 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
rp7410	2-8 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
rp7420	1-8 PA-8800 900 MHz-1.0 GHz	3 MB L1 32 MB L2	64 GB	Cell	PCI	HP-UX

rp7440	1-8 PA-8900 1.? GHz	3 MB L1 64 MB L2	128 GB	Cell	PCI-X	HP-UX
rp8400 rp8410	2-16 PA-8x00	depends	64 GB	Cell	PCI	HP-UX
rp8420	1-16 PA-8800 PA-8900 900 MHz-1.1 GHz	3 MB L1 32 MB L2 64 MB L2	256 GB	sx1000	PCI-X	HP-UX
rp8440	1-16 PA-8900 1.1 GHz	3 MB L1 64 MB L2	256 GB	sx2000	PCI-X	HP-UX

3.1.6 Itanium

HP produced three Itanium workstations before dropping Unix workstations completely, making these the last and probably fastest HP-UX workstations (that also run Windows!).

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
i2000	1-2 Itanium 733-800 MHz	*varies*	16 GB	82460GX	PCI, AGP	HP-UX, Linux, FreeBSD, Windows
zx2000	Itanium 2 900 MHz-1.5 GHz	*varies*	8 GB	zx1	PCI-X, AGP	HP-UX, Linux, FreeBSD, Windows, OpenVMS
zx6000	Itanium 2 900 MHz-1.5 GHz	*varies*	24 GB	zx1	PCI-X, AGP	HP-UX, Linux, FreeBSD, Windows, OpenVMS

HP also released a line of Itanium-based servers in the rack-mountable **Integrity rx** line.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
rx1600	1-2 Itanium 2 1.0 GHz	*varies*	16 GB	zx1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx1620	1-2 Itanium 2 1.3-1.6 GHz	*varies*	16 GB	zx1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2600	1-2 Itanium 2 1.0-1.5 GHz	*varies*	24 GB	zx1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2620	1-2 Itanium 2 1.3-1.6 GHz	*varies*	32 GB	zx1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx2660	1-2 Itanium 2 1.4-1.6 GHz	*varies*	32 GB	zx2	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx3600	1-2 Itanium 2 1.4-1.6 GHz	*varies*	192 GB	zx2	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx4610	2-4 Itanium 733-800 MHz	*varies*	64 GB	zx1	PCI	HP-UX, Linux, Windows
rx4640	1-4 Itanium 2 1.1-1.6 GHz	*varies*	64 GB	zx1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx5670	1-4 Itanium 2 1.3-1.5 GHz	*varies*	96 GB	zx1	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx6600	1-4 Itanium 2 1.4-1.6 GHz	*varies*	192 GB	zx2	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx7620	2-8 Itanium 2 1.1-1.5 GHz	*varies*	64 GB	SX1000	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx7640	2-8 Itanium 2 1.4-1.6 GHz	*varies*	256 GB	SX2000	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx8620	2-16 Itanium 2 1.1-1.6 GHz	*varies*	256 GB	SX1000	PCI-X	HP-UX, Linux, Windows, OpenVMS

rx8640	2-16 Itanium 2 1.4-1.6 GHz	*varies*	512 GB	SX2000	PCI-X	HP-UX, Linux, Windows, OpenVMS
rx9610	4-16 Itanium 733-800 MHz	*varies*	128 GB	AzuzA	PCI-X	HP-UX

3.1.7 VME and scientific

Integrated PA-RISC systems on VME boards, VXI boards and scientific systems, based on HP 9000/715 and B-Class workstations, used for medical, industrial and military data measurement and real time control.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
742i/50	PA-7100 50 MHz	128 KB	64 MB	ASP	VME	HP-UX, Linux, NetBSD, OpenBSD
742rt	PA-7100 50 MHz	128 KB	64 MB	ASP	VME	HP-RT
743i/64	PA-7100LC 64 MHz	256 KB	256 MB	LASI	GSC-M, PMC, VME	HP-UX, Linux, NetBSD, OpenBSD
V743/64 VXI E1497A	PA-7100LC 64 MHz	256 KB	128 MB	LASI	GSC-M, PMC, VXI	HP-UX, probably others
743i/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	GSC-M, PMC, VME	HP-UX, Linux, NetBSD, OpenBSD
743rt	PA-7100LC 100 MHz	256 KB	256 MB	LASI	GSC-M, PMC, VME	HP-RT
V743/100 VXI E1498A	PA-7100LC 100 MHz	256 KB	128 MB	LASI	GSC-M, PMC, VXI	HP-UX, probably others
744/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
744rt/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	GSC-M, PMC, VME	HP-RT
744/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
744/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	GSC-M, PMC, VME	HP-RT
745i/50	PA-7100 50 MHz	128 KB	128 MB	ASP	EISA, VME	HP-UX, Linux, NetBSD, OpenBSD
745i/100	PA-7100 100 MHz	512 KB	256 MB	ASP	EISA, VME	HP-UX, Linux, NetBSD, OpenBSD
745/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
745/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
747i/50	PA-7100 50 MHz	128 KB	128 MB	ASP	EISA, SGC, VME	HP-UX, Linux, NetBSD, OpenBSD
747i/100	PA-7100 100 MHz	512 KB	256 MB	ASP	EISA, SGC, VME	HP-UX, Linux, NetBSD, OpenBSD
748i/64	PA-7100LC 64 MHz	256 KB	256 MB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, NetBSD, OpenBSD

748i/100	PA-7100LC 100 MHz	256 KB	256 MB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, NetBSD, OpenBSD
748i/132L	PA-7300LC 132 MHz	128 KB	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
748i/165L	PA-7300LC 165 MHz	128 KB L1 512 KB L2	1 GB	LASI	EISA, PCI GSC-M, PMC, VME	HP-UX, Linux, OpenBSD
16600A Agilent	PA-7300LC 150 MHz	64 KB	160 MB	LASI	Channel probes, measurement, emulation	HP-UX LOGIC, probably others
16700A Agilent	PA-7300LC 150 MHz	64 KB	160 MB	LASI	Measurement, emulation	HP-UX LOGIC, probably others
16700B Agilent	PA-7300LC 150 MHz	64 KB	256 MB	LASI	Measurement, emulation	HP-UX LOGIC, probably others
16702A Agilent	PA-7300LC 150 MHz	64 KB	160 MB	LASI	Measurement, emulation	HP-UX LOGIC, probably others
16702B Agilent	PA-7300LC 150 MHz	64 KB	256 MB	LASI	Measurement, emulation	HP-UX LOGIC, probably others

3.1.8 Mainframe

These are large enterprise servers for computing and large databases, with a large range of expansion, CPUs, memory and storage options. Some could be clustered also.

Model	CPU	Cache	RAM	Design	Expansion	Operating systems
870	1-4 PCX 50 MHz	1 MB	1 GB	SPI	CIO	HP-UX
890	1-4 PA-7000? 60 MHz	4 MB	2.0 GB	Viper	HP-PB	HP-UX
T500	1-12 PA-7100 90 MHz	2 MB	3.75 GB	Viper	HP-PB	HP-UX
T520	1-14 PA-7150 120 MHz	2 MB	3.75 GB	Viper	HP-PB	HP-UX
T600	1-12 PA-8000 180 MHz	2 MB L1 8 MB L2	3.75 GB	Viper	HP-PB	HP-UX
V2200	4-16 PA-8200 200 MHz	4 MB	16 GB	HyperPlane	PCI	HP-UX
V2250	4-16 PA-8200 240 MHz	4 MB	16 GB	HyperPlane	PCI	HP-UX
V2500	2-32 PA-8500 440 MHz	1.5 MB	32 GB	HyperPlane	PCI	HP-UX
V2500 Cluster	4-128 PA-8500 440 MHz	1.5 MB	128 GB	HyperPlane	PCI	HP-UX
V2600	2-32 PA-8600 552 MHz	1.5 MB	32 GB	HyperPlane	PCI	HP-UX
V2600 Cluster	4-128 PA-8600 552 MHz	1.5 MB	128 GB	HyperPlane	PCI	HP-UX
Convex SPP1000/CD	2-16 PA-7100 100 MHz	2 MB	4 GB	Crossbar	SBus	SPP-UX
Convex SPP1000/XA	2-8 PA-7100 100 MHz	2 MB	2 GB	Crossbar	SBus	SPP-UX

Convex SPP1000/XA Cluster	8-128 PA-7100 100 MHz	2 MB	32 GB	Crossbar	SBus	SPP-UX
Convex SPP1200/CD	2-16 PA-7200 120 MHz	512 KB	4 GB	Crossbar	SBus	SPP-UX
Convex SPP1200/XA	2-8 PA-7200 120 MHz	512 KB	2 GB	Crossbar	SBus	SPP-UX
Convex SPP1200/XA Cluster	8-128 PA-7200 120 MHz	512 KB	32 GB	Crossbar	SBus	SPP-UX
Convex SPP1600/CD	2-16 PA-7200 120 MHz	2 MB	4 GB	Crossbar	SBus	SPP-UX
Convex SPP1600/XA	2-8 PA-7200 120 MHz	2 MB	2 GB	Crossbar	SBus	SPP-UX
Convex SPP1600/XA Cluster	8-128 PA-7200 120 MHz	2 MB	32 GB	Crossbar	SBus	SPP-UX
HP/Convex SPP2000 S-Class	4-16 PA-8000 180 MHz	2 MB	16 GB	Crossbar	PCI	SPP-UX
HP/Convex SPP2000 X-Class Cluster	8-512 PA-8000 180 MHz	2 MB	512 GB	Crossbar	PCI	SPP-UX
Superdome Legacy "white"	1-64 PA-8x00	varies	1TB	Cell	PCI-X	HP-UX, Linux
Superdome sx1000 "black"	1-64 PA-8800 PA-8900 Itanium 2	varies	2TB	SX1000	PCI X, PCIeX	HP-UX, Linux Windows, OpenVMS
Superdome sx2000 "black"	1-64 PA-8900 Itanium 2	varies	2TB	SX2000	PCI X, PCIeX	HP-UX, Linux Windows, OpenVMS
Stratus Continuum 400	4-8 PA-8500 PA-8600	1.5 MB	8 GB	Continuum	12 PCI	HP-UX, FTX
Stratus Continuum 600	4-8 PA-7100 PA-8000 PA-8500 PA-8600	0.5-2 MB	128-4 GB	Continuum	6 slots	VOS, FTX
Stratus Continuum 1200	4-16 PA-7100 PA-8000 PA-8500 PA-8600	0.5-2 MB	512-4 GB	Continuum	12-18 slots	VOS, FTX

3.2 HP 9000 and PA-RISC Story

3.2.1 PA-RISC in HP 9000

HP 9000 was a family of technical servers and workstations produced by HP between the 1980s and 2000s that included a diverse range of Unix computers, based on HP PA-RISC, Itanium and other architectures. Both RISC and Unix were developed into products during the 1980s, moving from academia via industrial R&D to productization — at a time when much computing was still done on mainframes, minicomputers and time-sharing machines such as DEC PDP, VAX, IBM AS/400 and System/360.

Table 3.11: PA-RISC computer period table

Period	Series	Classes
	Prelude: Early 1980s	
	Other HP 9000	200, 300, 500 series
I	Infancy: Late 1980s	
	HP 9000 800	Early 840 to 870, 600
	Other HP 9000	300, 400 series
II	Growth: 32-bit 1990s	
	HP 9000 700	Snakes 720/730/750
		Desktop 715/725
		Small 705/710
	HP 9000 800	F/G/H/I-Class
	Mainframes	890
	VME industrial	742, 745i, 747i
	Third party	PRO - Hitachi, NEC ...
III	Maturity: 1990s heydays	
	HP 9000 700	Pizzabox 712 and 715
	VME industrial	743, 744, 745, 748
	Portables	SAIC, RDI, Hitachi
	Visualize workstations	B-Class
		C-Class
		J-Class
	HP 9000 800	E-Class
	Lettered servers	A-Class
		D-Class, R-Class, K-Class
		L-Class and N-Class
		S-Class, X-Class Convex
		V-Class
	Mainframes	T-Class
IV	Decline: 2000s	
	Integrity	rp servers
	Itanium	rx servers
		Itanium workstations
	Mainframes	Superdome

HP 9000 and the PA-RISC series were HP's new line of products in that fledging market in the early 1980s. This page focuses on this PA-RISC part of that story, divided into four periods from the 1980s to the 2000s. A separate article is dedicated to the History of PA-RISC operating systems.

Prelude

In the early 1980s, HP worked on both Unix and RISC development and products. Before PA-RISC, the original HP 9000 series was released with the FOCUS-based 500 series (9020). In parallel, the Motorola 68000 were added as HP Unix workstations.

Infancy (I)

HP moved into the fledging "microcomputer" market in the late 80s with several differently positioned platforms. PA-RISC computers of the HP 9000 Series 800 were HP's RISC entry into that market. The other CISC HP 9000 offerings were sold by HP in parallel for almost a decade. The PA-RISC 9000 800 series were offered as servers initially for business applications, but were quickly adapted for technical and engineering. Several processor, fabrication and systems design were tried by HP in those late-1980s days with the 800s.

Growth (II)

Much of the growth and major developments of HP 9000 and PA-RISC happened in the early 1990s. To round up and segment its offerings, HP released a dedicated PA-RISC workstation line, the HP 9000 700 series. Based on the new, CMOS PA-RISC 1.1 processors, the original workstations consisted of the "Snake" 720/730/750, smaller systems (705/710) and technical desktops (715/725). They were often used as a platform for Unix-based graphics, engineering and R&D, and slowly became popular for high-end use cases. Some opening up of the tightly-controlled PA-RISC happened with the HP PRO organization and third-party systems.

Maturity (III)

Many products were released and the line-up matured during the 1990s, from small desktops to large server cabinets and mainframe-type computers, under increasing complex brands and series names — HP 9000 700, HP Visualize, HP Integrity with the various "lettered" workstations and server series A-Class, B-Class, J-Class and so on. PA-RISC moved from 32-bit to 64-bit with the revamped PA-8000 processors and its subsequent successors up to the Mako PA-8800 with fairly high-powered Unix systems for the niche HP-UX technical and business market. Commodity and mainstream alternatives to RISC and Unix slowly started to appear at the end of that era with Window NT, Linux and faster x86 computers.

Decline (IV)

HP slowly transitioned to a "post-RISC" phase in the 2000s, with a long-planned move to VLIW Itanium IA64 for its technical and Unix offerings. The decline of PA-RISC was set in stone much earlier than that, with the mid-1990s joint development of Itanium together with Intel, and decided in the mid-2000s. Beginning in the late 1980s, PA-RISC systems often wore the crown of fastest technical (RISC and Unix) workstations until the heydays of the 90s, albeit at a (boutique) price. PA-RISC was relegated in the 2000s to a niche market with the rp Integrity PA-RISC servers. As a result of a changing market environment, PA-RISC slowly was phased out of the technical HP line-up first for Itanium products and later for mainstream x86 (64-bit) computers.

3.2.2 HP 9000 800 servers

The original PA-RISC computers were the HP 9000 800 servers developed by HP in the 1980s and released in late 1980s. They consisted of several computers based on 32-bit PA-RISC 1.0 and 1.1 processors and different designs. System architecture was rather divergent to the 700s workstations with different chipsets, buses and I/O devices. HP 9000 700 series was introduced slightly later than the 800s, with a different, more workstation-centric focus.

- **Early 840 to 870**: The first PA-RISC systems to market were the early HP 9000/800 servers released between 1986 and 1990 on PA-RISC 1.0 processors. HP experimented with different concepts and designs for both computers and processors in that phase, from the TTL-based HP 9000/840 server in 1986 to the first CMOS-based HP 9000/842, 852, 865, 870 servers. First attempts were also made for lower-cost systems.
- The HP 9000/500 computers were the early-1980s predecessors of the PA-RISC workstations and started the HP 9000 series. They were based on a proprietary HP 32-bit processor — the HP FOCUS. First released in 1982, the HP 9000/520, originally 9020, was quickly followed by the HP 9000 530, 540 and 550 computers. Operating system support was limited to HP-UX which on HP FOCUS allegedly was the first commercial Unix supporting a multi-processor, multi-user system.
- There was a shortly-lived PA-RISC-based **HP 9000 600 series** in the late 1980s. The HP 90000/635SV and 645SV were supposedly server-only versions of the 800 series PA-RISC 1.0 HP 9000/835 and 845. Both were deskside server systems and ran HP-UX. The 600 series moniker was discontinued shortly after with servers taking the 800 and workstations the 700 series.
- **E-Class** and **F/G/H/I-Class**: These were the second generation HP 9000 800 servers from the early-1990s. The F/G/H/I-Class HP 9000 Nova servers share a similar, distinct 32-bit PA-RISC design. They had wildly diverse configurations for server applications from the small F10 to the large I70. The E-Class followed with the "low-cost" PA-7100LC processor and integrated system design in smallish tower cases with the E25 to the E55.

Due to their separate system design and usage scenarios, HP 9000 700 and 800 series used different HP-UX Unix versions for a long time, until HP-UX 10.20. Support for the 800 series in open source systems was always limited due to sparse documentation on their architecture. The 800 series PA-RISC servers carried on into the lettered servers of the A/D/K/N-classes that kept a divergent architecture to the 700 and Visualize workstations, focused on multi-user business applications.

3.2.3 HP 9000 700 workstations

A large range of PA-RISC workstations was sold by HP with the HP 9000 700 series, from the 1990s on. The 700 series soon became popular 32-bit Unix RISC workstations and used HP's new processors like the PA-7000, PA-7100 and PA-7100LC. At that time, much technical computing centered on Unix and RISC workstations, superseding older CISC computers. The new workstations were often used for CAD, CAM and specialized software for HP-UX or Unix. HP acquired Apollo Computers around the time, so the "Apollo" name and technology became part of some workstations, sometimes called "HP Apollo 9000."

- **Snakes 720/730/750**: The original HP 9000/720, 730 and 750 workstation computers were the first dedicated PA-RISC workstations on the PA-RISC 1.1 PA-7000 processor. They used rather large and heavy deskside and desktop cases with interlocking modules of backplanes and

I/O boards. The 730 and 750 were improved on a year later by the powerful PA-7100/PA-7150 powered HP 9000/735 and 755 workstations, among the fastest PA-RISC computers of the time.

- **Pizzabox 705/710**: The design of the original "Snake workstations" was integrated into smaller, pizza-box style desktop workstations with the HP 9000/705 and 710 with similar architecture but limited I/O and performance. The 705 and 710 were an early foray into pared-down "budget" workstations, with full functionality but compromises on performance and I/O, a concept revised later in mainstream PCs (and the HP 9000 712 workstations).
- **Desktop 715/725**: Soon after the original workstations, in 1991 a range of technical workstations was released with the PA-7100 and ASP based HP 9000/715 and HP 9000/725 in /33 (horrible) to /75 variants. These featured more standardized hardware and expandability and I/O options for technical users, packaged into a more "normal" desktop housing not dissimilar to contemporary PCs. They were rather popular.
- **Pizzabox 712 and newer 715**: PA-RISC computer design was updated in 1994 with the HP 9000/712 and newer 715 workstations, based on the modern, integrated PA-7100LC processor and LASI chipset. The 712 was a revolutionary pizza-box design that offered the advantages of a commercial Unix system on a RISC platform in a very small case (something Apple did a decade later again). Both were used for CAD and graphics, and were popular choiced for Unix and open source development.
- The first **PA-RISC portable**, SAIC Galaxy was developed as part of a military contract (TAC-4) by SAIC. It was based on the HP 9000 712 workstation mainboard, built into a ruggedized case for portable military applications.

PA-RISC 700 workstations gained wide popularity in engineering, industrial and academic fields during the 1990s. During that time, PA-RISC with the 700s workstations traded the "performance crown" of Unix and RISC computers frequently with DEC Alpha architecture.

3.2.4 VME and industrial

The **740s** VME-based PA-RISC computers were part of the HP 9000 700 series, sold from the early to late 1990s, used for industrial, scientific and military data measurement and real time control applications. These single-board computers utilized the industrial-grade VME bus for that. Processors included 32-bit PA-RISC PA-7100, PA-7100LC and PA-7300LC with HP LASI and ASP chipsets and some custom VME designs.

Operating systems were native HP-UX and HP-RT, the latter for real-time applications, with some supported in Open Source operating systems including Linux and BSD. They were used in a very wide variety of applications for industrial and scientific control and measurement, including by the US military.

- The **first-generation VME** computers from the early 1990s were PA-7100 ASP-based designs, the HP 9000/742i single-board computer, integrated into HP 9000/745i and 747i computers. They were closely based on the HP 9000 715 technical workstation, repackaged into single-board VME computers.
- Based on newer LASI and LC processors, the **second-generation VME**743i and 744 single-board computers were used in the ruggedized 745 and 748i computers. These in turn used the newer C-Class C132L Visualize workstations system design in a VME board.

- In addition to the VME boards, there were other industrial and measurement systems based on HP PA-RISC, which included the (HP) Agilent logic analyzers of the 16600A and 16700A series and also the HP/Agilent V743/64 (E1497A) and V743/100 (E1498A) VXI computers.

3.2.5 Third party

The **Precision RISC Organisation (PRO)** consortium was formed by HP and Convex in 1992 to promote the PA-RISC architecture. PA-RISC chips and designs were usually not sold to third-parties with licensing and distribution tightly controlled by HP to partners in the PRO. Some third party PA-RISC computers sold by PRO members as OEM in their markets, mostly Japan and Korea, during the mid-1990s were:

- Hitachi sold both indigenous workstations (3050RX) and servers (3500) with PA-RISC processors, and relabeled systems from HP as OEM (9000V). The Hitachi page has been updated to include information on more 3050RX workstations, 3500 servers and the OEM systems.
- Mitsubishi limited its PA-RISC line to the original HP 9000 "Snakes" (720, 730 and 750) sold in the early-1990s as "MELCOM ME RISC series"
- NEC sold a range of HP PA-RISC servers as OEM, mostly K, D, a L-Class
- OKI offered almost the whole range of HP PA-RISC servers and workstations in the 1990s with the various "OKITAC 9000 series."
- Samsung apparently also sold some rebadged HP 9000 700 workstations in Korea

3.2.6 Visualize Workstations

From the mid-1990s on, HP sold its PA-RISC workstations with lettered class names: the B, C and J-Class systems, still formally part of the 9000 700 series. Most of them were sold with "Visualize" branding indicating a focus on their preferred applications and use cases. They were were geared towards graphics and engineering applications such as CAD or CAM and often used with HP's powerful Visualize and Visualize-FX graphics adapters. Processors were almost the whole range of PA-RISC CPUs from 32-bit PA-7200 up to 64-bit PA-8900.

- **B-Class**: The entry-level and most common HP Visualize workstation during that era, the B-Class used desktop-type designs and streamlined system architecture, including the B132L, B1000 up to the B2600.
- **C-Class**: More powerful and better resourced HP Visualize workstations than the B-Class, the C-Class were still a desktop-type design with a slightly more sophisticated system architecture that included the C100, C132L, C240 up to the C3600 models.
- **J-Class**: Combining much of the PA-RISC architecture from the mid-90s to early-2000s, the HP Visualize J-Class workstations were a range of mini-tower computers with many options and designs, usually multi-processor capable, from the J200 to the J6000 and J7000.
- The first **PA-RISC laptop** was developed and release by RDI Tadpole as RDI PrecisionBook, a rare bird based on the Visualize C132L and C160L workstations.

3.2.7 Laptops and Portables

Only three portable PA-RISC workstations were produced during 1990s — all by third-party vendors utilizing HP 9000 workstation designs from that era. First, there was the military-focused SAIC Galaxy 1100 portable from 1994, based on HP 9000/712 workstations and available through the Navy TAC-4 program, a very rare computer. Then at the end of the decade, there were the RDI PrecisionBooks, true laptops based on C132L workstation designs from HP.

3.2.8 Lettered servers

In parallel to the workstations, HP 9000 servers were renamed with lettered designators and included a spectrum of different 32- and 64-bit PA-RISC computers. These servers were quite powerful at the time of the 1990s with diverse configurations and designs, from the small A-Class to the mid-size D-Class and cabinet-size K-Class. Also during that time, the system architecture between 700s workstations and 800s servers began to converge, only to start diverging again in the late-1990s with the Cell and Stretch architectures, when HP moved to hardware virtualization.

- **A-Class**: The first PA-RISC servers geared towards large-scale deployments into rack-space, the A-Class were small and use a streamlined system design specifically geared towards "Internet" applications (time of the dotcom boom). The HP 9000/A180 was a 32-bit PA-7300LC budget-oriented design similar to the HP Visualize B180L, while the HP A400 and A500 with a variety of 64-bit PA-8x00 processors were the early harbinger of the **rp** moniker with a similar architecture to the Visualize C3000/C3600 workstations.
- **D-Class**, **R-Class** and **K-Class**: Three groups of servers from the HP 9000 800 range that were all based on the premise of flexibility in system design, configuration and upgrades, and shared similar system designs from 32-bit PA-7100LC up to multi-processor 64-bit PA-8200. The tower-sized "enterprise" HP 9000 D-Class servers had up to two CPUs, eight hard-drives and eight I/O slots, from the entry D200 to the bigger D390. Built into a rack-mountable case, the HP 9000 R-Class R380 and R390 shared the D-Class platform with slight differences in I/O and storage.
- **L-Class** and **N-Class**: Rack-mountable 64-bit PA-RISC servers in two classes but in four different variants and system architecture, when HP experimented with designs and concepts for both PA-RISC and Itanium. Released between 1999 and 2002, the L1000 and L2000 were based on the Astro architecture used in workstations as well, the L1500, L3000 and N4000 on the Stretch chipset, a rather strange bird, with the later N4000 using the Cell crossbar chipset also used in the Superdome mainframe. These were already renamed into the **rp** category during their product lifecycle, in the rp5400 and rp7400 range.

3.2.9 Mainframes

The label "mainframe" is used rather broadly here to include all larger HP PA-RISC computers with a large amount of computing resources that were either multi-processor or cluster-type systems. Some were HP's own development, like the T-Class, an outgrow of the original 800 series servers, and the later Superdome, while others were either co-developed or acquired externally, like the SPP Exemplar architecture from Convex.

- **T-Class and 800s**: The HP 9000/T-Class servers were large 32-bit and 64-bit PA-RISC mainframes from the mid-1990s, built with modular system cards that contain processors, memory or I/O devices. The HP 9000/890 was an early iteration of the architecture, with the later

T500/T600 being updated sucessors. After the 64-bit T600 the basic system design of the T-Class was discontinued in favor of the more flexible Superdome systems.

- **S-Class and X-Class Convex**: The SPP Exemplar were cluster mainframes developed by Convex in the 1990s, based on a multi-processor system design with up to 128 PA-RISC 1.1 processors. Multiple types were available in the SPP1000, SPP1200 and SPP1600: compact systems, hypernodes and clusters. This was followed in 1997 with the 64-bit SPP2000 S-Class/X-Class, jointly marketed between HP and Convex. All these are based on a crossbar architecture with an internal switching component, based on GaA. The SPP Exemplar all ran Convex SPP-UX, a custom Mach-based Unix operating system.
- **V-Class**: The V-Class V2200, V2250 and V2500 and V2600 were the second generation scalable PA-RISC servers based on the Convex Exemplar architecture, with up to 32 64-bit PA-RISC processors in a single cabinet. The architecture was HP's own HyperPlane crossbar chipset, a continuation and upgraded from the original Convex GaA architecture with faster processors and memory. Individual V-Class nodes could be clustered into groups of four, connected by CTI links. Operating system was HP-UX.
- **Superdome**: The Superdome servers were a completely new design, for up to 64 processors per cabinet. The Superdome "Legacy" , or white systems, used a Cell crossbar chipset with 64-bit PA-RISC processors, while the newer Superdome sx1000 and sx2000, or black systems, used SX chipsets and a mixture of Itanium 2 processors. They all ran HP-UX and Linux, while the SX models also Windows and OpenVMS.

3.2.10 Integrity

HP renamed its PA-RISC servers again in the early 2000s into the **rp** series, and shifted the focus of PA-RISC more towards servers with that move. The rp servers were based on 64-bit PA-RISC processors from the PA-8500 to the PA-8800, all multi-processor. Only the first rp branded systems shared design features with contemporary workstations and older servers, while the rest were new, server-only designs.

- **rp2400**: A rebranding of the original **A-Class** 64-bit A400 and A500 servers as rp2400 to rp2470 2U rack-servers, that had one or two PA-RISC 2.0 processors in an Astro system design.
- **rp3400**: Successors to the popular rp2400 line, the rp3410 and rp3440 used the HP zx1 Itanium chipset for up to two PA-8800 or PA-8900 processors, also in a 2U case. Upgrades to Itanium were available.
- **rp4400**: Closely related to the rp3400 above, the rp4410 and rp4440 were 4U rack servers with up to four dual-core PA-8800 and PA8-900 on the HP zx1 chipset, released in 2004. Their design featured up to 128 GB memory and quite high memory data rate.
- **rp5400**: Again a rebranding, with the **L-Class** 64-bit servers including the rp5400 and rp5450 being the former L1000 and L2000 based on Astro/Elroy design, and the rp5430 and rp5470 the former L1500 and L3000 using the sophisticated Stretch chipset. These were again rack-mountable, in 7U, and had up to four processors.
- **rp7400**: Both a rebranding and redesign of the **N-Class** servers, the rp7400 was the original N4000 on a Strech chipset server, with the rp7405 and 7410 sharing the N4000 name but using a completely new, Superdome-like Cell design, for up to eight processors. Later versions include the rp7420 and rp7440 that supported even newer CPUs, expansion and more memory.

- **rp8400**: Some of the largest Cell-based 64-bit servers before the Superdome mainframe, the rp8400, rp8420 and rp8440 used up to sixteen processors up to the PA-8900 plus large amounts of expansion and RAM.

With the rp range HP moved its PA-RISC offering closer to the new Itanium architecture, which were called "rx." Product and technical design was similar between rp and rx, and the PA-RISC rp moved strongly towards Itanium design with the zx1 chipsets and upgrade paths to IA64 processors. The rp were the last line of PA-RISC servers.

3.2.11 Itanium

Around the turn of the century, HP started to offer servers and workstations based on Itanium IA64 technology, a VLIW architecture jointly designed with Intel. System architecture between the PA-RISC **rp** and IA64 **rx** servers converged with similar designs and chipsets. The zx1 chipset and Itanium buses were used and Itanium slowly phased out PA-RISC from HP's technical and Unix lineup, albeit at least half a decade later than originally planned.

- **rx Series**: A large variety of systems were available in parallel to their PA-RISC models to run either HP-UX, Linux, Windows or OpenVMS. Most of the rx are multi-processor systems, with many based on HP's own zx1 chipset, that was also used in PA-RISC systems, some using the zx2 and some the SX1000 and SX2000.
  A slew of systems were available, with the first generation based on zx1 including the 1U rx1600 and rx1620, the 2U rx2600 and rx2620, the 4U rx4640, the legacy 7U rx4610 and the 7U rx5670. These were followed soon by zx2 based systems, that were similar but offered more speed and newer Itanium 2 processors with the rx2660 and rx6600 servers, among others.
- **Itanium workstations**: Only three Itanium workstations were offered, the very early HP i2000 with a first-generation Itanium CPU and an Intel reference architecture, and the later, more flexible HP zx2000 and zx6000. The zx2000 had a sleek tower casing while the zx6000 was the dual-processor rack system. Both zx workstations were technically similar the the PA-RISC HP C8000 workstations and used the same HP zx1 platform. Itanium workstations were not a relevation performance-wise when compared to both earlier forecasts as well as to modern Intel x86 or even the last PA-RISC designs.

This was the end of the PA-RISC platform at HP, which vanished with diminishing market share until the mid-2000s. The process of the long decline of RISC and commercial Unix servers was already underway then, with Unix relegated to special applications and later to high-end, mission-critical servers. HP started withdrawing from Unix workstations before Itanium, but pared down its offering even further with the new CPU architecture. Shipments of Itanium workstations ceased two years after release, at the time when Intel moved the x86 architecture to 64-bit. Originally envisaged as an industry-changing architecture, Itanium ended up as alternative to other RISC platforms it was meant to replace, and marked the end-phase of HP Unix and RISC platforms.

On a side tangent of history, HP inherited both DEC Alpha RISC and OpenVMS through its acquisition of Compaq in the early 2002, both had been having rivals for HP platforms for decades. After discontinuing DEC Alpha, OpenVMS was to find a new home with the Itanium platform at HP, to which it was ported around 2005 to run on HP rx servers, being the first computers to offer both HP-UX and OpenVMS.

3.2.12 Other series

There were a few other computer series offered under the HP 9000 label before PA-RISC computers were released. This includes early Unix platforms from HP based on Motorola m68k CISC processors, the HP FOCUS line that preceeded PA-RISC and the HP 3000 minicomputers, that later switched to PA-RISC.

The **HP 9000 200 series** were the earliest incarnations of HP Unix platforms based on Motorola 68000, and started life as HP 9826 in 1981, all using the Motorola 68000 processor. Soon followed by other "high-end technical desktops" , such as the HP 9836, 9816, 9920, 9817 and 9837H, there series was renamed in the early 1980s to HP 9000 200 series, and the individual computers to, for example HP 9000/220 (for the 9920). The 200s also ran versions of HP-UX Unix.

The other series based on Motorola M68k processors was the **HP 9000 300 series**, sold from the mid-1980s to the early 1990s and also a Unix platform. The 300s had a new, functional design with several distinct boxes for each computer, a design later taken over for the first HP 9000 700s series workstations. The 300 series used Motorola CISC processors from the 68010 up to the -40. Besides HP-UX, the 300 series were supported by a variety of BSD operating systems from the 1980s well into the 2010s, including the mythical 4.4BSD and the OpenBSD/hp300 and NetBSD/hp300 siblings.

Related to the 300 series but incorporating technology from the 1989 acquisition of Apollo Computers, the **HP 9000 400 series** were based on Motorola 68030 and 68040 processors and ran HP-UX and Domain/OS (Apollo Unix). The 400 series were sold in parallel to PA-RISC computers of the 700 and 800 series in the early 1990s, and were widely supported by BSD and open source operating systems. Many designs, devices and peripherals were shared between the Motorola 68000-based 400 series and the PA-RISC 700 and 800 series, including the SGC and EISA buses, SCSI controllers, HP-HIL and HP-IB peripherals, graphics adapters.

The **HP 3000** line were the HP business minicomputers, first released in 1972, with their own operating system MPE, application stack and distinct customer base. From the late 1980s on, HP 3000 moved to the PA-RISC platform and used systems that were closely based on the HP 9000 800 series. HP 3000 used PA-RISC actually earlier than the widely-popular HP 9000 700 workstation series. The first MPE for PA-RISC release was MPE/XL, the last MPE version was MPE/iX with limited Unix support and POSIX compliance. HP 3000 and MPE have been discontinued since. For more information read the 3000-MPE (Software) article from hpmuseum.net and The History of the HP 3000 from Bob Green.

3.2.13 About

This page is an attempt to unify all the different leads and streams of HP 9000 and PA-RISC into a single story, but simplifications were made. The information on this page is based mostly on existing OpenPA content, but also includes new content and interpretation of other sources. Some pieces were sourced from the great HP Computer Museum, but also from news releases, journals or HP Labs communication.

For release dates of HP 9000 computers and their entry prices, there is also the PA-RISC Timeline page. A tabular overview of HP 9000 PA-RISC systems is on the main PA-RISC Computers section that links to pages with more details for individual systems. The history of PA-RISC processors and system architecture is covered briefly in the PA-RISC Hardware page.

The history of PA-RISC operating systems merits its own article. Four main streams of systems are covered — commercial Unix, open source, research projects, and others. Release dates and versions are in more detail on the PA-RISC Timeline.

3.2.14 References

- HP Computer Museum Australia, 2021
- The Alpha 21264: NT's Greatest RISC, Windows NT Magazine / December 1998
- Ten catastrophes: All-time worst tech industry executive decisions, ZDNet September 2011
- Itanium: A cautionary tale, CNet December 2005
- The Battle in 64 bit Land, 2003 and Beyond, Real World Tech, 2003
- The Last Itanium, At Long Last, Next Platform, May 2017
- HP Completes Its PA-RISC Road Map With Final Processor Upgrade, Information Week, June 2005

3.3 HP 9000/705 and 710

3.3.1 Overview

The HP 9000/705 and HP 9000/710 were the first small PA-RISC workstations and miniaturized versions of the "Snakes" 720, 730 and 750. The technical architecture was taken over taken over with some significant changes:

- Smaller I/D caches
- Lower CPU clock rate
- Different connection to the memory subsystem
- Integration of graphics, SCSI, Ethernet subsystem onto a single mainboard
- Reduced expansion possibilities

The HP 9000 710 workstation was introduced by HP in 1992 for a list price of $7,490.

3.3.2 System

CPU

- 705: PA-7000 35 MHz with 96 KB off-chip L1 cache
- 710: PA-7000 50 MHz with 96 KB off-chip L1 cache

Chipset

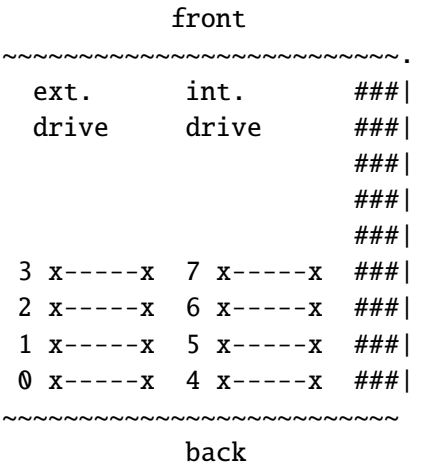
- ASP chipset
- Viper memory and I/O controller, low-cost version implemented in two chips
- NCR 53C700 8-bit single-ended SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller
- Audio 8-bit mono PSB2160 CODEC
- Other I/O (serial, parallel, i8042)

Buses

- PBus processor/memory bus, 200 MB/s at 50 MHz (710), 140 MB/s at 35 MHz (705)
- VSC main system bus, 100 MB/s at 25 MHz (710), 70 MB/s at 17.5 MHz (705)
- GSC system-level I/O bus
- SCSI-2 narrow single-ended bus

Memory

- HP-proprietary 72-pin SIMMs
- Eight sockets
- 16 MB (4×4) minimum, 64 MB maximum
- Memory has to installed in *quartets*:
  first in the "even" slots (0, 2, 4, 6), then in the "odd" slots (1, 3, 5, 7):



Expansion

- No expansion slots

Drives

- SCSI 3.5âĂş 50-pin Narrow SE hard drive
- SCSI half-height 5.25âĂş 50-pin Narrow SE drive, external accessible

3.3.3 External

- SCSI-2 50-pin single-ended
- Two Serial RS232C DB9
- Parallel DB25
- 15-pin AUI 10 Mbit & 10Base2 BNC Ethernet
- VGA HD15
- HP-HIL connector for input devices
- Two phone jacks (microphone, headphones)

3.3.4 Operating systems

- HP-UX
  - 10.20
  - 11.00: could work, but unsupported and slow
- Linux
- OpenBSD

3.3.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
705	21.9	33.0		
710	31.6	47.6	0.99	1.44

3.3.6 References:

Articles

- High-Performance Design for Low-Cost PA-RISC Desktops (.pdf) pp. 56-63 Craig Fink et al (August 1992: Hewlett-Packard Journal)

3.4 HP 9000/712

3.4.1 Overview

The HP 9000 712 workstations were a new, "low-cost" approach from HP for PA-RISC workstations, and the second "pizza-box" sized system after the 705 and 710 workstations.

The design goal from HP for the 32-bit HP 9000/712 workstation was to reach performance levels of 1992-era workstations and servers such HP 9000 735 workstation, at a fraction of their fabrication costs. Everything is rather simplified and small, the case is one of the smallest Unix workstation cases, similar to the Sun SPARCstation 10 and 20 cases.

The 712 became hugely popular in the 1990s in technical disciplines as well as in graphics, software and early (90s!) multi-media development. Especially the 712/60 was competitively priced during that time as an entry-level RISC Unix system, compared both the HP offerings as well as Unix RISC computers from the competition. It was one of a breed of pizza-box computers of that era and later on sold also well on hobbyist markets.

Model	Introduced	Price
712/60	1994	$4,400
712/80	1994	$8,820
712/100	1995	$15,100

The HP 9000 712 and its architecture was the basis for other systems — the newer, LASI-based 715 workstations were very similar, the SAIC Galaxy 1100, the first PA-RISC portable, was based on it as well as some measurement and control computers, such as the Agilent HP 16505A Prototype Analyzer. In the US Navy TAC-4 program for tactical computers from the mid-1990s, the HP 9000 712 was used widely as "TAC-4 Desktop Computer" throughout the US Navy and military vessels, together with other PA-RISC systems from the TAC-4 contract.

3.4.2 System

CPU

- 712/60: PA-7100LC 60 MHz with 1 KB on-chip L1 and 64 KB off-chip L1 cache
- 712/80: PA-7100LC 80 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 712/100: PA-7100LC 100 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache

Chipset

- LASI integrated chipset
- (Integrated) NCR 53C710 8-bit single-ended SCSI-2
- (Integrated) Intel 82596CA 10 Mbit Ethernet controller
- (Integrated) Harmony CD/DAT quality 16-bit stereo audio
- Artist graphics, 8-bit
- (Integrated) Other I/O (serial, parallel, Flopyy)

Buses

- GSC system level I/O bus (128 MB/s)
- SCSI-2 single-ended bus

Memory

- 72-pin ECC SIMMs
- Takes 8-32 MB modules
- Either 4 memory sockets, on 712/60 and /80 models, or 6, on 712/100
- 16 MB minimum, 128 MB/192 MB maximum
- Memory has to be installed in pairs, starting from slot 0, the closest slot to the drives.

Expansion

- VRAM expansion slot for:
  - A2263-66520M - Video RAM expansion for higher resolutions/more colors
- One slot for a GIO card, a special formfactor GSC bus card only used in the 712, with the following cards available:
  - A2878A - second video
  - A4011A - 8025 Token Ring interface
  - A4011B - 8025 Token Ring interface
  - A4013A - second serial port
  - A4014A - second Ethernet LAN (AUI+TP) and serial port.
  - A4015A - second serial *&* X25 link
  - A4217A - second Ethernet LAN (AUI+TP) *&* second VGA
  - TAMS 50488 - HP-IB interface
- One slot for a TSIO card, a special formfactor GSC card for the *Teleshare* expansion slot, with only one card offered:
  - A4012A - Teleshare POTS interface with two RJ11C jacks

Drives

- SCSI 3.5âĂş Fast-Narrow SE 50-pin hard drive
- 3.5âĂş Floppy drive with special connector

3.4.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- Serial RS232C DB9, up to 115200 baud
- Parallel DB25
- Ethernet RJ45
- Ethernet AUI 15-pin
- VGA HD15
- Two PS/2 connectors for keyboard & mouse
- Three phone jacks (microphone, headphones and line-in)

3.4.4 Operating systems

- HP-UX
  - 10.20
  - 11.00 and 11i v1: 32-bit supported but slow
- NeXTSTEP (the NeXTSTEP PA-RISC port was designed for the HP 9000 712)
- Linux
- OpenBSD
- NetBSD

3.4.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp	SPEC95*rate*, int	SPEC95*rate*, fp
712/60	67.0	85.3	2.08	2.66	18.7	23.9
712/80	97.1	123.3	3.12	3.55	28.1	32.0
712/100	117.2	144.2	3.76	4.06	33.8	36.3

3.4.6 Dimensions

Height	Width	Depth	Weight
70mm	432mm	400mm	8kg

3.4.7 References

Manuals

- Model 712 Technical Reference (PDF, 3.7 MB, Hewlett Packard 1995)
- Model 712 Service Handbook (PDF, 4.4 MB, Hewlett Packard 1995)

Articles

- HP 9000 Model 712 Overview (PDF, HP Journal 4/95)
- Design of the Model 712's I/O subsystem (LASI) (PDF, HP Journal 4/95)
- Product design of the Model 712 (PDF, HP Journal 4/95)
- In addition to the above almost the whole HP Journal April 1995 Issue deals with the 712 workstation.
- Product Brief HP 9000 Models 712/60, 712/80, and 712/100 Workstations (PDF, 88 KB, Hewlett Packard)
- First NeXT RISCWorkstation: Our first look at NEXTSTEP on HP's low-cost pizza box, NeXTWORLD, April 1994

ROM update

There is an firmware update available for the 712, which contains the latest version 2.3.

- PF_C7120023.txt has details about the contents and installation of the patch.
- PF_C7120023 contains the patch.

Other

- NetBSD 712 serial console HOWTO, instructions to configure 712s to use serial console (*i.e.*, run headless)
- Pinout for the AUI/RS232 Y-cable for the optional second Ethernet/serial card.

3.5 HP 9000/715

3.5.1 Overview

The HP 9000/715 were technical PA-RISC workstations from HP from the early 1990s, powerful, expandable HP-UX systems that were often used for technical design, CAD/CAM and engineering. Different configurations were available in two different 715 versions:

- The HP 9000 715/33, 715/50 and 715/75 were the first 715 series with PA-7100 processors and the original HP ASP chipset.
- The HP 9000 715/64, 715/80, 715/100 and 715/100XC were more modern and based on the LASI chipset design, technically close to the HP 9000 712 workstations.

Model	Introduced	Price
715/33	1992	$4,995
715/50	1992	$11,895
715/64	1994	$10,000
715/80	1994	$13,000
715/100	1994	$19,000
715/100XC	1995	$21,000

3.5.2 System

CPU

- 715/33: PA-7100 33 MHz with 128 KB off-chip L1 cache
- 715/50: PA-7100 50 MHz with 128 KB off-chip L1 cache
- 715/64: PA-7100LC 64 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 715/75: PA-7100 75 MHz with 512 KB off-chip L1 cache
- 715/80: PA-7100LC 80 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 715/100: PA-7100LC 100 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 715/100XC : PA-7100LC 100 MHz with 1 KB on-chip L1 and 1024 KB off-chip L1 cache

Chipset

715/64, 80 and 100

- LASI chipset, integrated
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Wax for EISA bridge, HP-HIL
- Artist graphics, 8-bit

- Other I/O like serial, parallel, HP-HIL, Floppy

715/33, 50 and 75

- ASP chipset
- Viper memory and I/O controller
- NCR 53C700 8-bit single-ended SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller
- Intel 82350 EISA bus adapter chipset (EISA to GSC)
- CRX graphics, 8-bit
- Audit 16-bit CS4215 CODEC
- Other I/O (serial, parallel, i8042)

Buses

- GSC system level I/O bus
- EISA additional expansion I/O bus
- SCSI-2 single-ended narrow bus
- *715/33, 55, 75*PBus processor/memory bus
- *715/33, 55, 75*VSC main system bus
- *715/33, 55, 75*SGC expansion of the mainbus to the SGC expansion card

Memory

- 72-pin ECC SIMMs
- Eight sockets for 8-32 MB modules
- *715/33* 6 memory sockets
- 16 MB to 192 MB (6×32) or 256 MB (8×32) supported

Expansion

- *715/33, 55, 75* One slot for SGC (EISA formfactor) cards
- *715/64, 80, 100* One slot for GSC (EISA formfactor) cards
- With a special HP adapter EISA cards can be used in the GSC or SGC slots

Drives

- Two SCSI 3.5âĂș Fast-Narrow SE 50-pin hard drives
- SCSI half-height 5.25âĂș Fast-Narrow SE 50-pin drive, externally accessible

3.5.3 External

- SCSI-2 50-pin single-ended Fast-Narrow
- Two Serial RS232C DB9 (up to 115200 baud)
- Parallel DB25
- Ethernet AUI 15-pin
- VGA HD15
- *715/33, 55, 75* HP-HIL connector for input devices
- *715/64, 80, 100* SMD-10 connector, to connect HIL and PS2
- Four phone jacks (microphone, headphones and line-in and ?)

3.5.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1 (the last two only on 64, 80 and 100)
- NeXTSTEP
- Linux
- OpenBSD
- NetBSD

3.5.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
715/33	32.5	52.4	1.01	1.58
715/50	49.2	78.8	1.53	2.46
715/64	80.6	109.4	2.52	3.31
715/75	82.6	127.2	2.51	3.85
715/80	96.3	123.2	3.01	3.50
715/100	115.1	138.7	3.76	4.06
715/100XC	132.2	184.6	4.55	4.70

3.5.6 References

Manuals

- Model 715 Service Handbook (PDF, 5.1 MB, Hewlett Packard 1995)

ROM update

There is a firmware update available for the 715/64, /80 and /100.

- C7X50016.text has details about the contents and installation of the patch.
- C7X50016.frm contains the new firmware.

3.6 HP 9000/720, 730 and 750

3.6.1 Overview

The HP 9000 720, 730 and 750 computers were the first PA-RISC workstations, called the *Snakes*, based on the first 32-bit PA-RISC 1.1 processors. They were built into solid cases consisting of interlocking exchangeable modules ("sliders"). The storage subsystem has its own "slider", connected to the main I/O board with a short external cable. The 720 and 730 share the same backplane and I/O board and can be upgraded through the exchange of the CPU board. Later HP 9000/735 workstations share a similar system setup and 720/730 CPU and I/O boards can be swapped *together* for 735 boards, and vice versa (as 735 I/O boards do not work with 720 CPU boards, both boards have to be exchanged).

The HP 9000 720, 730 and 750 were used by the US Navy as part of the TAC-3 (Tactical Advanced Computer) for a variety of applications, including electronic intelligence gathering (ELINT).

Model	Introduced	Price
720	1991	$11,990
730	1991	$
750	1991	$52,890

3.6.2 System

CPU

- 720: PA-7000 50 MHz with 384 KB off-chip L1 cache
- 730: PA-7000 66 MHz with 384 KB off-chip L1 cache
- 750: PA-7000 66 MHz with 512 KB off-chip L1 cache

Chipset

- ASP chipset
- Viper memory and I/O controller
- NCR 53C700 8-bit single-ended SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller
- Intel 82C501AD Ethernet transceiver
- Intel 82350 EISA bus adapter chipset (EISA to GSC)
- Other I/O (serial, parallel, i8042)

Buses

- PBus processor/memory bus at processor clock
- VSC main system bus at 0.5 of processor clock

- GSC system-level I/O bus
- EISA additional I/O expansion bus
- SGC expansion of the mainbus to the SGC expansion cards
- SCSI-2 narrow single-ended bus

Memory

- HP proprietary memory modules, some shared with 735/755
- 720: 8 slots
- 730: 8 slots and 16 MB onboard
  272 MB (8×32+16) maximum
- 750: 12 slots
  768 MB (12×64) maximum

Expansion

- 720/730:
  - One SGC (DIO-II formfactor) expansion slot
  - Sne EISA slot
- 750:
  - Two SGC (DIO-II formfactor) expansion slots
  - Four EISA slots

Drives

- 720/730: Two SCSI 3.5âĂş Narrow SE 50-pin hard drives
- 750: Two SCSI half-height 5.25âĂş Narrow SE 50-pin SCSI drives and two SCSI full-height 5.25âĂş Narrow SE 50-pin SCSI drives

3.6.3 External

- SCSI-2 50-pin single-ended
- Two Serial RS232C DB9 (up to 115200 baud)
- Parallel DB25
- 15-pin AUI 10 Mbit & 10Base2 BNC Ethernet
- Graphics depend on installed SGC framebuffer
- HP-HIL connector for input devices
- Jack for beep audio

3.6.4 Operating systems

- HP-UX10.20, 11.00 (unsupported)
- Linux
- OpenBSD
- NetBSD

3.6.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
720	36.4	58.2	1.20	2.00
730	47.8	75.4	1.50	2.30
750	48.1	75.0	1.50	2.30

3.6.6 References:

Manuals

- HP Apollo 9000 Model 720/730 owner's guide (PDF, 1.8 MB, Hewlett Packard)
- HP Apollo 9000 Model 750 owner's guide (PDF, 2.1 MB, Hewlett Packard)

Articles

- Midrange PA-RISC Workstations with Price/Performance Leadership (.pdf) pp. 6-11 Andrew J. DeBaets and Kathleen M. Wheeler (August 1992: Hewlett-Packard Journal)

3.7 HP 9000/725

3.7.1 Overview

The HP 9000 725 PA-RISC workstations from 1992 were the designated smaller replacements for the HP 9000 750 servers while still offering the same amount of I/O options. They are technically based on their 715 workstations counterparts.

3.7.2 System

CPU

- 725/50: PA-7100 50 MHz with 128 KB off-chip L1 cache
- 725/75: PA-7100 75 MHz with 512 KB off-chip L1 cache
- 725/100: PA-7100LC 100 MHz with with 1 KB on-chip L1 and 256 KB off-chip L1 cache

Chipset

725/50 and 725/75

- ASP chipset
- Viper memory and I/O controller
- NCR 53C700 8-bit single-ended SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller
- Intel 82C501AD Ethernet transceiver
- Intel 82350 EISA bus adapter chipset (EISA to GSC)
- Other I/O (serial, parallel, i8042)
- CRX graphics, 8-bit
- Audit 16-bit CS4215 CODEC

725/100

- LASI chipset
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Other I/O (serial, parallel, i8042)
- Wax chip (EISA bridge, HP-HIL)
- Artist graphics, 8-bit
- Other I/O (serial, parallel, Floppy controller, HP-HIL)

Buses

- GSC system-level I/O bus
- EISA additional I/O expansion bus
- *725/50, 725/75*: PBus processor/memory bus
- *725/50, 725/75*: VSC main system bus
- *725/50, 725/75*: SGC expansion of the mainbus to the SGC expansion card
- SCSI-2 single-ended narrow bus (Fast on *725/100*)

Memory

- *72*-pin ECC SIMMs
- Takes 8-32 MB modules
- Eight sockets
- 32 MB (2×16) minimum, 256 MB (8×32) maximum

Expansion

- *725/50, 725/75*: Three EISA expansion-slots,
  One slot for either a SGC (*EISA formfactor*) or EISA card.
- *725/100*: One EISA expansion slot,
  Three slots for either GSC (*EISA formfactor*) or EISA cards.

Drives

- One tray for one 3.5âĂş Narrow SE 50-pin SCSI hard drive
- One tray for one 3.5âĂş Floppy drive
- Two trays for one half-height 5.25âĂş Narrow SE 50-pin SCSI drive each, externally accessible

(*725/100* supports Fast-Narrow drives)

3.7.3 External

- SCSI-2 50-pin Narrow SE single-ended (Narrow-fast on *712/100*)
- Two Serial RS232C DB9
- Parallel DB25
- Ethernet AUI 15-pin
- VGA HD15
- *725/50, 725/75*: HP-HIL connector for input devices

- 725/100: SMD-10 connector, to connect HIL/PS2 with a special adapter
- Four phone jacks (microphone, headphones, line-in and ?)

3.7.4 Operating systems

- HP-UX10.2011.00 and 11i v1 (unsupported on 50 and 75)
- NeXTSTEP
- Linux
- OpenBSD
- NetBSD

3.7.5 Benchmarks

Model	SPEC95, int	SPEC95, fp
725/50	1.53	2.46
725/75	2.51	3.85
725/100	3.76	4.06

3.8 HP 9000/735 and 755

3.8.1 Overview

Project names:

The HP 9000 735 and 755 were powerful technical and graphical PA-RISC workstations from the early 1990s. They use 32-bit PA-RISC 1.1 PA-7100 or PA-7150 processors — the latter in the fast (and expensive) 735/125 and 755/125 configuration. Both 735 (desktop) and 755 (tower) have a solid and heavy desk-side case built with separate modules for I/O and CPU. These boards, along with EISA cages and the storage subsystem are built into so-called "sliders" that can be removed separately from the system. They support a large set of I/O buses, expansion options and drives. The 735 was widely used as a FDDI node in Convex clusters and as 735/125 one of the fastest RISC workstations running NeXTSTEP.

The 735 and 755 have similar cases to their PA-7000 predecessors HP 9000/730 and 750.

Model	Introduced	Price
735/99	1992	$37,395
735/125	1992	
755/99	1992	$58,995
755/125	1992	

3.8.2 System

CPU

- PA-7100 99 MHz with 256/256 KB off-chip I/D cache
- PA-7150 125 MHz with 256/256 KB off-chip I/D cache

Chipset

- ASP2 chipset
- Viper memory and I/O controller
- *Cutoff* ASIC, interfacing with memory (*Viper*) and I/O buses, provides address decoding, bus arbitration and interrupts
- *Shortstop* ASIC, coordinates data communication between the I/O buses and the mainbus
- NCR 53C700 8-bit single-ended SCSI-2
- NCS 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller
- AMD Formac Plus Am79C830 FDDI controller
- Other I/O (serial, parallel, i8042)
- Intel 82350 EISA bus adapter chipset (EISA to GSC)

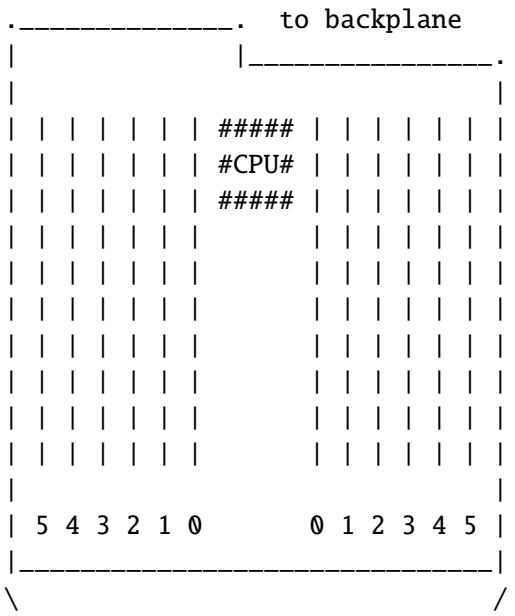
- Audio 16-bit CS4215 CODEC

Buses

- PBus processor/memory bus, 66 MHz on 735/99 and 755/99 (264 MB/s)
- VSC main system bus
- GSC system-level I/O bus
- EISA additional I/O expansion bus
- SGC expansion of the mainbus to the SGC expansion cards
- SCSI-2 narrow single-ended bus
- SCSI-2 Fast-Wide *high-voltage differential* (HVD) main storage I/O bus

Memory

- HP proprietary memory modules, same as 720, 730 and 750, and the Nova servers
- 8-32 MB modules
- *755* supports 64 MB modules
- 12 sockets
- *735* 16 MB onboard, 400 MB maximum
- *755* 768 MB maximum
- Memory has to be installed in pairs, from bank 0 to the outside



Expansion

- *735*:
  - One SGC in DIO-II formfactor
  - One EISA slot
  - One special daughter card slot for:
    - A2665A - FDDI SAS daughter card with MIC connector
    - A2658A - AUI Ethernet daughter card
    - A2831A - ThinLAN Ethernet daughter card
- *755*:
  - Two SGC slots in DIO-II formfactor
  - Four EISA slots

Drives

- *735*: one tray for either two 3.5âĂş SCSI 68-pin Fast-Wide HVD or 50-pin narrow SE hard drives.
- *755*: one tray for two half-height 5.25âĂş SCSI drives and two trays for one full-height 5.25âĂş SCSI drive each

3.8.3 External

- SCSI-2 50-pin single-ended external
- SCSI-3 68-pin Fast-Wide *high-voltage differential* HVD external
- Two standard RS232C serial
- DB25 parallel
- *735* 15-pin AUI or 10Base2 BNC Ethernet or FDDI SAS MIC connector
- *755* 15-pin AUI & 10Base2 BNC Ethernet connectors
- RGB BNC, depends on installed framebuffer, if at all
- HP-HIL connector for input devices
- Five phone jacks (microphone, headphones, line-in, line-out and speaker)

3.8.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1 (both unsupported)
- NeXTSTEP
- Linux

- OpenBSD
- NetBSD

3.8.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95*rate*, int	SPEC95*rate*, fp
/99	3.22	4.06	29.4	35.8
/125	3.97	4.61	36.3	40.9

3.8.6 References

Manuals

- HP Apollo 9000 Series 700 Model 735 Workstations (PDF, 7.6 MB, Hewlett Packard 1992)

3.9 HP 9000/742i VME Workstation

3.9.1 Overview

The HP 9000/742i *Sidewinder* were VME-based PA-RISC single-board computers (SBCs) based on the HP 9000 715/50 workstation integrated onto a single board with fewer expansion possibilities. SCSI is routed through the VME-P2 connector at the back of the board. Since the board features a VME controller it is able to talk to other VME devices on the same bus and control them.

The HP 742rt version of these VME computers was designed for the HP-RT realtime operating system.

3.9.2 System

CPU

- PA-7100 50 MHz with 128 KB off-chip L1 cache

Chipset

- ASP chipset
- NCR 53C700 8-bit single-ended SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller
- Viper memory and I/O controller
- Intel 82350 EISA bus adapter chipset (EISA to GSC)
- CRX graphics, 8-bit
- CS4215 CODEC for 16-bit stereo audio
- VME bus adapter
- Other I/O (serial, parallel, i8042)

Buses

- PBus processor/memory bus
- VSC main system bus
- GSC system-level I/O bus
- VME bus
- SCSI-2 narrow single-ended bus.

Memory

- 72-pin ECC SIMMs
- Takes 8-32 MB modules
- Two slots
- 16 MB (2×8) minimum, 64 MB (2×32) maximum

Expansion

- None

3.9.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- Two Serial RS232C DB9
- Parallel DB25
- DB15 Ethernet AUI 15-pin

3.9.4 Operating systems

- HP-UX: 9.01 to 10.20
- Linux: should run
- 742rt: HP-RT realtime operating system

3.9.5 Benchmarks

Model	SPEC95, int	SPEC95, fp
742i/50	1.53	2.46

3.9.6 Dimensions

Height	Width	Depth	Weight	Power
40mm	233mm	160mm	0.9kg	35W @ 5V DC

3.9.7 References

Manuals

- HP 9000 Model 742i Owner's Guide (PDF, 0.5 MB, Hewlett Packard 1993)

3.10 HP 9000/743i and 744 VME Workstation

3.10.1 Overview

The HP 9000 743i and 744 PA-RISC workstations are VME single-board computers (SBCs) for use in VME mainframes, based on HP 9000/715 (743i) and HP Visualize B132L/B160L workstations (744). The SPU system processing unit is integrated with memory and several I/O controllers onto a single-height 2U VME board.

The 743i and 744 SBCs had a few on-board expansion options with GSC-mezzanine (GSC-M) and PCI-mezzanine (PMC) cards. Installed into a VME cage that provides power and VME bus connection, the SBCs could talk to and control other VME cards on the same VME bus.

VME workstations

The 743i boards are used in the HP 9000 748i industrial workstations, the 744 boards in the HP 9000 745 and 748 industrial workstations.

US Navy TAC

The 743i and 744 VME computers were used by the US Navy through the TAC program (Tactical Advanced Computer), in which HP was contracted to supply several PA-RISC computers. They were used in several tactical display and control applications, including the AN/UYQ-70 workstation aboard surface as well as submarine vessels and surveillance aircraft. Utilizing third-party VME devices and integration, especially for graphics, the 743i/744 were used with FDDI networking in these roles.

HP-RT workstations

The HP 743rt and 744rt version of these VME computers were designed for the HP-RT realtime operating system.

Agilent VXI

The HP/Agilent V743/64 (E1497A) and V743/100 (E1498A) VXI embedded computers are apparently very close to the 743i VME single board computers. The V743 was a 1-Slot, C-size, message-based computer with direct VXI access that ran HP-UX and supported C-SCPI and Agilent VEE.

3.10.2 System

CPU

- 743i/64: PA-7100LC 64 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 743i/100: PA-7100LC 100 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- V743/100 VXI: PA-7100LC 100 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 744/132L: PA-7300LC 132 MHz with 128 KB on-chip L1 cache

- 744/165L: PA-7300LC 165 MHz with 128 KB on-chip L1 and 512 KB off-chip L2 cache

Chipset

- LASI integrated chipset
- (Integrated) NCR 53C710 8-bit single-ended SCSI-2
- (Integrated) Intel 82596CA 10 Mbit Ethernet controller
- (Integrated) Harmony CD/DAT quality 16-bit stereo audio
- Wax EISA bridge
- Dino GSC-to-PCI bridge
- 744: Phantom PseudoBC GSC+ port
- 744: Visualize-EG "Graffiti" graphics with 2MB frame buffer memory
- CS4215 or AD1849 programmable CODECs
- VME controller
- PCMCIA controller
- (Integrated) Other I/O (serial, parallel, Floppy)

Buses

- GSC bus
- Optional EISA bus
- Optional PCI-32/33 bus
- VME bus
- SCSI-2 Fast-Narrow single-ended bus

Memory

- 743i: 8 – 256 MB RAM, with four slots for 8-64 MB special ECC mezzanine cards
- 744: 16 – 1025 MB RAM, with four slots for 16-256 MB special ECC mezzanine cards
- V743 VXI: 32 – 128 MB RAM
- 743i and 744 use different memory cards

Expansion

Some pins of the P2-VME connector are used to route GSC bus traffic to expansion options, VME cages need to be properly jumpered to support this to not interfere with these transfers. The 743/744 boards must not be used in VXI cages since some of the VXI pins carry voltage which would result in damaged devices on the GSC bus.

- GSC bus expansion, through HP extender cards
- PCI and PCMCIA connector, through HP extender cards
- Expansion options for devices via expansion adapters:
  - Two GSC-mezzanine (GSC-M) cards, with the A4219A GSC Expansion kit that occupies one VME slot
  - Two PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board that occupies one VME slot
  - Two additional PCI-mezzanine (PMC) cards, requires PMC bridge adapter that occupies another VME slot
  - The PMC and GSC adapter cannot work together
- VME connection
- V743 VXI: VXI connection (TTL, ECL trigger buses)

3.10.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- Two Serial micro-RS232C DB9[1]
- Micro-DB25 parallel[1]
- Micro-DB15 Ethernet AUI 15-pin[1]
- Micro-DB15 VGA graphics[1]
- Two PS/2 connectors for keyboard & mouse
- Micro-DB9 for audio breakout[1]
- V743 VXI: GPIB

Notes

1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

3.10.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- OpenBSD
- 743rt and 744rt: HP-RT realtime operating system

3.10.5 Benchmarks

Model	SPEC95, int	SPEC95, fp
743i/64	2.52	3.31
743i/100	3.76	4.03
744/123L	6.45	6.70
744/165L	7.90	7.64

3.10.6 References

- HP 9000 Model 743 Owner's Guide (PDF, 1.8 MB, Hewlett Packard 1997)
- 743, 744 and 748 Technical Reference Manual for OEMs (PDF, 2.2 MB, Hewlett Packard 1997)
- 744 Owner's Guide (PDF, 1.4 MB, Hewlett Packard 1997)
- HP Model 748 Service Handbook (.pdf, 3.6 MB, Hewlett Packard 1997)
- 743 Service Handbook (Hewlett Packard, URL gone)
- Installing the A4505A PCI Module Upgrade (Hewlett Packard, URL gone)
- Installing the A4504A PMC Bridge Adapter and A4509A Expansion Adapter (Hewlett Packard, URL gone)
- Installing Model 743 RAM Boards (Hewlett Packard, URL gone)
- Installing Model 744 RAM Cards (Hewlett Packard, URL gone)
- VME Services for HP-UX 10 and 11 (Hewlett Packard, URL gone)
- Navy pursues "network-centric" vision for shipboard electronics (Military&Aerospace Electronics: March 1998)
- Agilent E1498A V743/100 VXI Embedded Computer - Datasheet (Agilent Technologies: 2001)

3.11 HP 9000/745 VME Workstations

3.11.1 Overview

The HP 9000 745 PA-RISC industrial computers are HP 9000 744 VME boards in a heavy VME case, which provides the neccessary I/O facilities:

- Room for up to four SCSI devices, which can be accessed from the outside
- Four-slot EISA or PCI cage
- Room for PCI-mezzanine expansion cards, via special PMC bridges/expansion

3.11.2 System

CPU

- 745/132L: PA-7300LC 132 MHz with 128 KB on-chip L1 cache
- 745/165L: PA-7300LC 165 MHz with 128 KB on-chip L1 and 512 KB off-chip L2 cache

Chipset

- LASI chipset
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Wax EISA bridge
- Dino GSC-to-PCI bridge
- Phantom PseudoBC GSC+ port
- Visualize-EG "Graffiti" graphics with 2MB frame buffer memory
- VME "Backplane controller ASIC"
- Harmony CD/DAT quality 16-bit stereo audio
- PCMCIA controller
- Other I/O (serial, parallel, HP-HIL)

Buses

- GSC bus
- Optional EISA bus
- Optional PCI-32/33 bus
- VME bus
- SCSI-2 Fast-Narrow single-ended bus

Memory

- 16-256 MB special ECC mezzanine cards (same as for the 744 VME boards)
- Up to four cards can be installed
- 16 MB minimum, 1 GB maximum amount of RAM

Expansion

- Two sites for GSC-mezzanine (GSC-M) cards, requires the A4219A GSC Expansion kit **or**
- Two sites for PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board (two additional PMC sites can be obtained through the addition of the A4509A PMC Expander board to the above). The PMC bridge/expander boards connect to the VME backplane on a VME slot above the 744 processing board. However they probably use the GSC bus routed through the VME P1/P2 connectors, and not the VME bus.
- Either four EISA or four PCI (5 V) slots in a separate I/O cage

Drives

- Four bays for external-accessible SCSI (SCSI-2 Single-ended) drives
- One bay for a 3.5âĂş SCSI drive

3.11.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- Two Serial micro-RS232C DB9[1]
- Micro-Parallel DB25[1]
- Micro-DB15 Ethernet AUI 15-pin[1]
- Micro-DB15 VGA graphics[1]
- Two PS/2 connectors for keyboard & mouse
- Micro-DB9 for audio breakout[1]

Notes

1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

Other

- Refer also to the 743i and 744 VME boards description

3.11.4 Operating systems

- HP-UX 10.20, 11.00 and 11i v1
- Linux
- OpenBSD

3.11.5 Benchmarks

Model	SPEC95, int	SPEC95, fp
745/123L	6.45	6.70
745/165L	7.90	7.64

3.11.6 Dimensions

Height	Width	Depth	Weight	Power
177mm	425mm	412mm	29kg	400W

3.11.7 References

Manuals

- HP Model 745 Technical Reference Manual (.pdf, 1.7 MB) Hewlett Packard (April 1999)
- Model 745 Industrial Controller Owner's Guide (.pdf, 4.8 MB) Hewlett Packard (November 1999)
- Model 745 Service Handbook (.pdf) Hewlett Packard (November 1999)

3.12 HP 9000/745i and 747i VME Workstations

3.12.1 Overview

The HP 9000/745i and 747i were VME computers and one of the first PA-RISC workstations from HP for industrial and medical use. They are technically close to the HP 9000 715 and 725 workstations but integrated into (U) rack-mountable cases. They run standard PA-RISC operating systems.

The CPU and I/O controllers are integrated on a VME single board computer (SBC) which is identical on 745i and 747i. The 747i are built with a bigger case and feature VME expansions slots, the 745i do not.

Both have a HP-IB interface for controlling, measurements and instrumentation. These machines have two pairs of LED banks, one at the front and the other directly on the CPU board on the back.

3.12.2 System

CPU

- 745i/50: PA-7100 50 MHz with 128 KB off-chip L1 cache
- 747i/50: PA-7100 50 MHz with 128 KB off-chip L1 cache
- 745i/100: PA-7100 100 MHz with 512 KB off-chip L1 cache
- 747i/100: PA-7100 100 MHz with 512 KB off-chip L1 cache

Chipset

- ASP chipset, featuring:
- Viper memory and I/O controller
- NCR 53C700 8-bit single-ended SCSI-2
- Intel 82596DX 10 Mbit Ethernet controller
- Intel 82350 EISA bus adapter chipset
- CRX graphics, 8-bit
- HP-IB controller
- 747i: VME controller
- PSB2160 CODEC for 8-bit mono audio
- Other I/O (serial, parallel, i8042)

Buses

- PBus processor/memory bus
- VSC main system bus

- GSC system-level I/O bus
- EISA I/O expansion bus
- HP-IB bus (IEEE-488); peripheral bus
- SCSI-2 narrow single-ended bus
- *747i*: SGC expansion of the mainbus to the SGC expansion slot
- *747i*: VME bus

Memory

- 72-pin ECC SIMM
- 8-32 MB modules (/100 models take 64 MB modules)
- Four sockets
- /50 models: 16 MB (2×8) minimum, 128 MB (4×32) maximum
- /100 models: 16 MB (2×8) minimum, 256 MB (4×64) maximum

Expansion

- *745i*:
  - Four EISA expansion slots
- *747i*:
  - Two EISA expansion slots
  - One SGC (*DIO-II formfactor*) expansion slot
  - Six VME slots

Drives

- One bay for an external-accessible 5.25âĂş half-height SCSI drive
- One bay for an external-accessible 3.5âĂş SCSI drive or floppy
- One bay for a 3.5âĂş SCSI drive

3.12.3 External

- SCSI-2 50-pin single-ended
- Two Serial RS232C DB9
- Parallel DB25
- Ethernet AUI 15-pin
- HD 15 VGA

- HP-HIL connector for input devices
- HP-IB for peripherals
- Three phone jacks (microphone-in, headphone-out and speaker-out)

3.12.4 Operating systems

- HP-UX10.20 and 11.00
- NeXTSTEP
- Linux
- OpenBSD

3.12.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
/50	36	72	1.53	2.46
/100	81	138	3.22	4.06

3.12.6 Dimensions

Model	Height	Width	Depth	Weight	Power
745i	175mm	425mm	412mm	18.6kg	350W
747i	310mm	425mm	412mm	29kg	700W

3.12.7 References

Manuals

- 745i/50, 745i/100, 747i/50, and 747i/100 Owner's Guide (.pdf, 1.7 MB) Hewlett Packard (August 1993: First edition)

3.13 HP 9000/748i and 748 VME Workstations

3.13.1 Overview

The HP 9000 748i and 748 ruggedized PA-RISC workstations are HP 9000 743i and 744 VME boards in a heavy VME-case, which provides the neccessary I/O facilities:

- Six 6U VME slots for additional I/O boards
- Room for up to four SCSI devices, which can be accessed from the outside
- Four-slot EISA or PCI cage

3.13.2 System

CPU

- 748i/64: PA-7100LC 64 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 748i/100: PA-7100LC 64 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- 748/132L: PA-7300LC 132 MHz with 64/64 KB on-chip L1 cache
- 748/165L: PA-7300LC 165 MHz with 64/64 KB on-chip L1 and 512 KB off-chip L2 cache

Chipset

- LASI ASIC, which features:
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Wax EISA bridge
- Dino GSC-to-PCI bridge
- 748: Phantom PseudoBC GSC+ port
- 748: Visualize-EG "Graffiti" graphics with 2MB frame buffer memory
- Harmony CD/DAT quality 16-bit stereo audio
- VME controller
- PCMCIA controller
- Other I/O (serial, parallel)

Buses

- GSC bus
- Optional EISA bus
- Optional PCI-32/33 bus

- VME bus
- SCSI-2 Fast-Narrow single-ended bus

Memory

- 748i and 748 use different cards
- 748i: 8-64 MB special ECC mezzanine cards
- 748: 16-256 MB special ECC mezzanine cards
- Up to four cards
- 748i: 8 MB minimum, 256 MB maximum amount of RAM
- 748: 16 MB minimum, 1 GB maximum amount of RAM

Expansion

- Two sites for GSC-mezzanine (GSC-M) cards, requires the A4219A GSC Expansion kit **or**
- Two sites for PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board (two additional PMC-sites can be obtained through the addition of the A4509A PMC Expander board to the above)
- Six 6U VME slots
- Either four EISA or four PCI slots in a separate I/O cage

3.13.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- Two Serial micro-RS232C DB9[1]
- Micro-Parallel DB25[1]
- Micro-DB15 Ethernet AUI 15-pin[1]
- Micro-DB15 VGA graphics[1]
- Two PS/2 connectors for keyboard & mouse
- Micro-DB9 for audio breakout[1]
- On configurations with an EISA cage: HIL connector

Notes

1. These micro-connectors need HP conversion cables to provide the normal-sized versions of their respective connectors

3.13.4 Operating systems

- HP-UX 10.20, HP-UX 11.00 and 11i v1
- Linux
- OpenBSD

3.13.5 Benchmarks

Model	SPEC95, int	SPEC95, fp
748i/64	2.52	3.31
748i/100	3.76	4.03
748/123L	6.45	6.70
748/165L	7.90	7.64

3.13.6 Dimensions

Height	Width	Depth	Weight	Power
324mm	425mm	419mm	29kg	2×350W

3.13.7 References

Manuals

- Model 748 Workstation Owner's Guide (PDF, 3.2 MB, Hewlett Packard 1997)
- 743, 744 and 748 Technical Reference Manual (PDF, 2.2 MB, Hewlett Packard 1997)
- HP Model 748 Service Handbook (.pdf, 3.6 MB, Hewlett Packard 1997)

Other

- Refer also to the 743i and 744 workstations

3.14 HP 9000 74x Expansion

3.14.1 743i and 748i (/64 and /100) RAM

Used in:

- 743i/{64,100}
- 748i/{64,100}

HP parts:

- A4263A - 8 MB RAM card
- A4264A - 16 MB RAM card
- A4265A - 32 MB RAM card
- A4266A - 64 MB RAM card

3.14.2 744, 745 and 748 (/132L and /165L) RAM

Used in:

- 744/{132L,165L}
- 745/{132L,165L}
- 748/{132L,165L}

Faster versions of the above 743i/748i ECC mezzanine cards.

Original HP part numbers:

- A4501A - 16 MB RAM card (only supported in HP-RT)
- A4502A - 32 MB RAM card
- A4503A - 64 MB RAM card
- A4449A - 128 MB RAM card
- A6005A - 256 MB RAM card

3.14.3 Cables

Breakout cables for the micro-connectors found on the 743i and 744 VME boards. These cables convert the micro-output to the regular connectors.

- HP A4300A HP Parallel: High Density 25-pin to standard 25-pin (female)
- HP A4301A RS-232C: High Density 9-pin to standard 9-pin (male)
- HP A4302A Audio: High Density 9-pin to three mini jacks

- HP A4303A LAN: High Density 15-pin to 15-pin AUI
- HP A4305A Video for EVC monitors: High Density 15-pin to EVC 35-pin connector (female)
- HP A4223A Video: High Density 15-pin to standard 15-pin (female)
- HP C2955A SCSI: High Density 50-pin to High Density 50-pin, .5m (male)

3.14.4 GSC-M cards

GSC-M cards are special mezzanine versions of expansion cards for the GSC bus.

- A4267A - 8-plane graphics
- A4268A - Fast-Wide *high-voltage differential* (HVD) SCSI
- A4315A - HCRX-8 graphics
- A4316A - HCRX-24 graphics
- J3420A - ATM card

3.15 HP 16600 and 16700 Agilent Logic Analyzers

3.15.1 Overview

The HP 16600A and 16700A are logic analyzers with PA-RISC processors sold by HP and Agilent, based on PA-RISC HP 9000 workstation architecture from the mid-1990s. These were the successors to the Agilent 16500 series analyzers and used in engineering and science for measurements, logic analysis, prototyping and verification. All variants are based on the same 16700A or 16700B main logic board built into different chassis' with the system architecture probably related to the B132L/B160L workstations with some custom I/O hardware and buses.

- **16600A**: Small base system with integrated channel probes, one measurement slot and one emulation slot.
- **16700A**: Base system in a modular frame, with five measurement slots and two emulation slots.
- **16700B**: Updated 16700 base system with modular frame and faster mainboard and components.
- **16701A/16701B**: An "expansion frame" to extend the 16700 series systems with space for five more measurement and two more emulation slots.
- **16702A**: Same system board as the 16700 in a compact case as integrated Logic Analysis System with 10.3″ 800x600 LCD screen display. With five measurement slots and two emulation slots.
- **16702B**: Updated version of the integrated 16702A with faster mainboard and components and a different case with integrated 12.1″ touch screen. It lost the integrated keyboard on the front and one emulation slot at the back for an integrated CD drive.

Model	Introduced	Price
16600A	1998	$10,040-$25,740
16700A	1998	$9,990
16700B	2000	
16702A	1999	$11,500
16702B	2000	$11,990

In electronics and microprocessor design, these systems were able to analyze various buses (AGP, ISA, CAN, PCI, HP-PB, SCSI, USB, DIMM memory and many others) and emulate microprocessor families (ARM, IBM PowerPC, Pentium, Motorola PowerPC and MPC, CPU32, M-core, Toshiba, MIPS, Intel 960, Motorola 68000 and 88000 and many others).

Another Agilent PA-RISC product, the HP **16505A** Prototype Analyzer was a standard HP 9000 712 workstation that connected to an Agilent 16500A series logic analyzer via special hardware and software. Around 2004, Agilent moved away from PA-RISC and HP-UX to Windows-based logic analyzers.

3.15.2 System

The 16600 and 16700 series are designed around the following system design with individual boards:

- **CPU board**: The main logic board houses the PA-RISC processor, main ASICs, memory, backplanes and system slots.

- **PCI board**: Bridges the PCI backplane from the CPU board to the instrument backplane for measurement modules. Extends the I/O circuitry from the CPU board and connects the Interface board
- **Interface board**: Distributes the signals from CPU and PCI boards throughout the system and connects to the measurement backplane, to which the measurement and emulation modules connect
- **Module interface board**: Connects the measurement and emulation slots and buses to the Interface board
- **Expansion frame**: Extends the measurement backplane into a separate frame with more slots.

CPU

- PA-7300LC 150 MHz with 64 KB on-chip L1 cache

Chipset

- LASI integrated chipset
- (integrated) NCR 53C710 8-bit single-ended SCSI-2
- (integrated) Intel 82596CA 10 Mbit Ethernet controller
- (integrated) Harmony CD/DAT quality 16-bit stereo audio
- Dino GSC-to-PCI bridge
- Phantom PseudoBC GSC+ port
- (probably) Visualize-EG onboard graphics with 2 MB frame buffer memory (4 MB with the performance option 003)
- 30 MHz on-board crystal oscillator VCK
- PLL clock distribution IC
- Various ICs for the bridges and measurement and emulation ports
- FPGA1 (16700 BP protocol) on the PCI board
- FPGA1 (instrument BP protocol) on the PCI board
- Serial EPROM on the PCI board
- Intercard-controller on the Interface Board
- PLL, expansion frame cicuitry, clock distribution on the Interface board

Display

- *16702A* Integrated 10.3″ 800×600 LCD display
- *16702B* Integrated 12.1″ 800×600 LCD touch panel
- All could optionally be ordered with a VGA monitor

- Supported 1280×1024 VGA monitor, 1600×1200 with option 003

Input

- The 16702 series had build in input keys and devices
- *16702A* Integrated front-panel keyboard
- *16702B* Touch screen, knobs and dedicated hot keys

Buses

- GSC bus
- Optional PCI-32/33 bus for I/O devices and the measurement and emulation modules
- IMB Inter-Module bus
- Protocol bus
- Measurement Module Backplane, Agilent 16500-compatible, connects via IMB, protocol bus to the interface board
- Emulation Module Interface, connects via IMB, protocol bus to the interface board
- SCSI-2 Fast-Narrow single-ended bus

Memory

- All logic analyzers had factory installed RAM that could be upgraded with factory options
- 120-pin memory expansion boards
- Apparently some memory is onboard
- *16700A and 16702A* 64 MB to 160 MB internal RAM (with performance option 003)
- *16700B and 16702B* 128 MB to 256 MB internal RAM (with performance option 003)

Expansion

- 16700A/16700B and 16702A/16702B expansion slots:
  - Five measurement module slots
  - Two emulation module slots
  - *16702B* Only one emulation module slot
- 16600A expansion options:
  - One measurement module slot
  - One emulation module slot
  - Channel probes on the front

  - 16600A: 204 channels
  - 16601A: 136 channels
  - 16602A: 102 channels
  - 16603A: 68 channels
- 16701A and 16701B expansion slots, requires 16700 or 16702:
  - Five measurement module slots
  - Two emulation module slots

Drives

- SCSI 3.5âĂş Fast-Narrow SE 50-pin hard drive for a factory-installed internal SCSI disk
- 3.5âĂş Floppy drive
- *16700A/16702A* 4 GB SCSI drive
- *16700B/16702B* CD-ROM drive
- *16700B/16702B* 9 GB SCSI drive

3.15.3 External

- Ethernet LAN RJ45 and BNC
- *16702B* 100BaseTX (Fast-Ethernet)
- SCSI-2 50-pin single-ended
- Serial RS232C DB9
- Parallel DB25
- VGA monitor
- Two PS/2 connectors for keyboard and mouse
- Target Control Port
- Port IN and Port OUT
- *16700/16702* Connector for 16701A expansion frame

3.15.4 Operating systems

- HP-UX with HP LOGIC and Agilent software
- They might run Linux and OpenBSD but not sure (the hardware is similar to already supported systems)

3.15.5 Options

The 16600 and 16700 series could be ordered with factory options.

Table 3.33: HP Agilent 16600 and 16700 factory options

Option	16600A	16700A/16702A	16700B/16702b
001	17″ 1280x1024 monitor	17″ 1280x1024 monitor	17″ 1280x1024 monitor
003	160 MB system RAM, 4 MB video RAM	160 MB system RAM, 4 MB video RAM	256 MB system RAM, 4 MB video RAM
004	External CD-ROM drive	External CD-ROM drive	
008		18 GB external SCSI drive	18 GB external SCSI drive
009			External removable hard drive
010	Two 17-channel probe leads		
012			Multiframe module

3.15.6 References

- Great series of articles on HP 16700A logic analyzer from "Keith" (2013: techtravels.org)
- Agilent Technologies 16700A/16702A Service Guide (PDF) (2000: Agilent Technologies Company)
- 16700 Series Logic Analysis System Product Overview (PDF) (2003: Agilent Technologies)
- HP 16600A and 16700A Series Logic Analysis System Mainframes Procuct Overview (PDF) (1998: Hewlett-Packard Company)
- Installation Guide HP 16600A Seriesi HP 16700A HP 16702A Measurement Modules (PDF) (1999: Hewlett-Packard Company)
- Agilent Technologies 16700B and 16702B Logic Analysis Systems (PDF) (2003: Agilent Technologies)
- Processor and Bus Support for Agilent Technologies Logic Analyzers (PDF) (2001: Agilent Technologies)
- Don't be illogical when choosing logic-analysis tools Dan Strassberg (1999: EDN Network)
- HOT PRODUCTS OF 1998: Part 3 (1998: EDN Network)

3.16 HP 9000/A180

3.16.1 Overview

The HP 9000 A-Class A180 and A180C were among the last 32-bit PA-RISC HP 9000 800 servers, in a small and rack-mountable case. Designated "Enterprise Internet Servers" they were geared towards deployment in rack-space in datacenters and thus do not have video output, only serial console and a web console. System design was pretty pared down and streamlined, with a simplified 32-bit PA-RISC design not dissimilar to the HP Visualize B180L workstation, minus the graphics and a few of the I/O devices.

Model	Product	Introduced	Price
A180	A5182A	1998	
A180C	A5183A	1998	$16,000

3.16.2 System

CPU

- A180: PA-7300LC 180 MHz with 64/64 KB on-chip I/D L1 cache
- A180C: PA-7300LC 180 MHz with 64/64 KB on-chip I/D L1 and 1 MB off-chip L2 cache

The additional 1 MB L2 cache is the only difference between both systems. It was upgradeable through two DIMM slots near the CPU.

Chipset

- LASI chipset
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Dino GSC-to-PCI bridge
- Phantom PseudoBC GSC+ port
- DEC 21142/43 10/100BaseT PCI Ethernet
- Other I/O (serial)

Buses

- GSC+ general system-level I/O bus (probably clocked at 36 MHz — 144 MB/s peak data rate)
- PCI high performance device I/O bus
- SCSI-2 Fast-Narrow single-ended; main storage I/O bus

Memory

- 72-pin ECC EDO SIMMs, 60ns or faster.
- Takes 64-256 MB modules
- Eight slots
- 128 MB (2×64) minimum, 2048 MB (8×256) maximum

Expansion

- Two slots for either GSC (*EISA formfactor*) or PCI cards

Drives

- One tray for two 3.5âĂş Fast-Narrow 50-pin SCSI hard drives

3.16.3 External

- SCSI-2 50-pin single-ended
- Serial RS232C DB9
- Fast Ethernet RJ45
- Ethernet RJ45 "Web Console"

3.16.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- OpenBSD
- NetBSD

3.16.5 Benchmarks

Model	SPEC95, int	SPEC95, fp
A180	?	?
A180C	9.22	8.60

3.16.6 References

Manuals

- A180 User's Manual (PDF, 0.9 MB)

◈ HP's HP9000 A-Class A180C Enterprise Server - Designed as a low-cost, high-density Web server, is the A-Class as mean as it is lean? Ralph Barker at *Dr. Dobb's* (June 1999, accessed December 2017)

3.17 HP A400, A500 (rp2400)

3.17.1 Overview

The HP A-Class servers rp2400/rp2430/rp2405 (A400), and rp2450/rp2470/rp2405 (A500) are the early 2000s 64-bit successors of the popular HP 9000/A180 rack servers. Still being part of the HP 9000 800 series, the A-Class were renamed to the **rp** server series. The A400 was single-processor while the A500 was SMP-capable and had better expandability. The rp2405 was a low-cost version, introduced two years later based on similar hardware to the A500 that could be upgraded to a rp2470.

System design is based on 64-bit PA-RISC processors with large on-chip L1 caches, Astro memory/CPU controller and Elroy PCI bridges for expansion and I/O, a similar but simplified architecture of the HP Visualize C3000 line of workstations.

Model	rp	Product	Introduced	Price
A400	rp2400	A6109AA6109B	2000	
A400	rp2430	A6889A	2000	
(A400)	rp2405	A7121A	2002	
A500	rp2450	A5570AA5570B	2000	
A500	rp2470	A6890A	2000	
(A500)	rp2405	A7122A	2002	

3.17.2 System

CPU

The A400 servers were uniprocessor while the A500 were up to two-way SMP.

Model	CPU	Processor options
A400/rp2400	1	-44: PA-8500 440 MHz with 512/1024 KB on-chip I/D L1 cache -5X: PA-8600 550 MHz with 512/1024 KB on-chip I/D L1 cache
A400/rp2430	1	-6X: PA-8700 650 MHz with 768/1536 KB on-chip I/D L1 cache
A400/rp2405	1	-6X: PA-8700 650 MHz with 768/1536 KB on-chip I/D L1 cache
A500/rp2450	1-2	-44: PA-8500 440 MHz with 512/1024 KB on-chip I/D L1 cache -5X: PA-8600 550 MHz with 512/1024 KB on-chip I/D L1 cache
A500/rp2470	1-2	-6X: PA-8700 650 MHz with 768/1536 KB on-chip I/D L1 cache -7X: PA-8700 750 MHz with 768/1536 KB on-chip I/D L1 cache
A500/rp2405	1-2	-6X: PA-8700 650 MHz with 768/1536 KB on-chip I/D L1 cache

The following -8X or -9X might have been shipped or were theoretically upgradable.

- -8X: PA-8700 875 MHz with 768/1536 KB on-chip I/D L1 cache each

- -9X: PA-8800 (dual-core) 900 MHz/1.0 GHz with 1.5/1.5 MB on-chip L1 and 32 MB off-chip L2 cache each

Chipset

- Astro memory/Runway controller, connects to the system/processor bus (1-2 CPUs), dedicated memory bus and to the I/O systems via five (A400) or seven (A500) I/O links
- A400: Three Elroy PCI bridges (LBAs), convert the five I/O links from Astro into three PCI buses
- A500: Four Elroy PCI bridges (LBAs), convert the seven I/O links from Astro into four PCI buses
- Two HP Diva Serial [GSP] Multiport UARTs
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C876 SCSI controller, (includes two Symbios Logic 53C875 cores with each one Ultra-Wide SCSI-2 bus)
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Runway CPU/memory bus, 120 MHz
- 1.9 GB/s system bus bandwidth
- 1.9 GB/s memory bandwidth
- SCSI-2 Ultra-Narrow single-ended bus
- Two SCSI-3 Ultra2-Wide LVD buses
- *A400* Three independent PCI-64/66 I/O buses on five 250 MB/s I/O links
- *A500* Four independent PCI-64/66 I/O buses on seven 250 MB/s I/O links

Memory

- ECC SDRAM DIMMs, 256 MB/512 MB/1 GB modules
- Eight slots, A400 uses only four
- *A400* 2 GB maximum
- *A500* 8 GB maximum

Expansion

- *A400* Two PCI 64-bit/66 MHz, 5 V slots
- *A500* Four PCI 64-bit/66 MHz, 5 V slots

Drives

- Two trays for each one 3.5âĂş Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector which require a special spud to be plugged into the system.

3.17.3 External

- SCSI-2 50-pin Ultra-Narrow single-ended
- SCSI-3 68-pin Ultra2-Wide LVD
- DB25 male RS232C serial for console/UPS (a break-out cable which converts to three DB9 plugs)
- Fast Ethernet RJ45
- Ethernet RJ45 for Secure Web Console/GSP

3.17.4 Operating systems

- HP-UX: 64-bit 11.00, 11i v1 and 11i v2
- Linux

3.17.5 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000*rate*, int	SPEC2000*rate*, fp
A500-5X(rp2450)	422	414	2-CPU: 9.3	2-CPU: 7.6
A500-7X(rp2470)	581		6.74 2-CPU: 12.9	

3.17.6 Dimensions

Model	Height	Width	Depth	Weight
	95mm	482mm	635mm	23kg
Rack-mounted	2U	482mm	774mm	23kg

3.17.7 References

Manuals

- hp server rp2400 series whitepaper (URL gone)
- hp server rp2405 series whitepaper (URL gone)
- rp24xx Hardware Manual (URL gone)

Website

- Doug's HP 9000 - GSP Notes Page with a detailed description of the available GSP commands.

3.18 HP Visualize B132L, B160L, B180L

3.18.1 Overview

The HP Visualize B-Class B132L, B160L and B180L were entry-level HP 9000 PA-RISC workstations introduced in 1997. Based on 32-bit PA-RISC processors, they were the successors to the popular 715 Unix workstations with improved performance and I/O options. The B-Class were developed together with the C-Class workstations C132L/C160L, having similar design but more integrated functionality on the mainboard and fewer expansion options to minimize cost.

Model	Number	Introduced	Price
B132L	9000/778	1996	$10,480
B160L	9000/778	1996	$16,480
B180L	9000/778	1997	$16,500

The **+**-models B132L+ and B180L+ had faster Ultra-Wide SE SCSI and 100 Mbit Ethernet instead of Fast-Wide HVD SCSI and 10 Mbit Ethernet.

3.18.2 System

CPU

- B132L: PA-7300LC 132 MHz with 64/64 KB int. L1 (+ 1 MB ext. L2)
- B132L+: PA-7300LC 132 MHz with 64/64 KB int. L1 (+ 1 MB ext. L2)
- B160L: PA-7300LC 160 MHz with 64/64 KB int. L1 (+ 1 MB ext. L2)
- B180L+: PA-7300LC 180 MHz with 64/64 KB int. L1 (+ 1 MB ext. L2)

The external L2 cache SRAM is optional and installed in two DIMM slots below the CPU socket. The modules must be of equal size. Usually, these systems come with two 512 KB modules, totalling in 1 MB L2.

Chipset

- LASI chipset
- Phantom PseudoBC GSC+ port
- NCR 53C710 8-bit single-ended SCSI-2
- *B132L, B160L*NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- *B132L+, B180L+*Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- *B132L+, B180L+* DEC 21142/43 (*Tulip*) Fast-Ethernet controller
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Wax EISA bridge
- Dino GSC-to-PCI bridge

- Visualize-EG ("Graffiti") graphics with 2MB frame buffer memory
- Other I/O (serial, parallel, Floppy)

Buses

- GSC general system-level I/O bus
  - B132L and B132L+: 33 MHz 132 MB/s
  - B160L: 40 MHz 160 MB/s
  - B180L+: 36 MHz 144 MB/s
- EISA additional expansion I/O bus
- PCI-32/33 high-performance device I/O bus
- SCSI-2 Fast-Narrow single-ended bus
- *B132L, B160L*SCSI-2 Fast-Wide *high-voltage differential* main storage I/O bus
- *B132L+, B180L+*SCSI-2 Ultra-Wide single-ended main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Six slots for 16-256 MB modules
- 32 MB to 1.5 GB supported

Expansion

- B132L, B160L:
  - One slot for a GSC (EISA formfactor) or PCI 32-bit/33 MHz, 3.3 V card
  - One slot for a GSC (EISA formfactor) or PCI 32-bit/33 MHz, 3.3 V or EISA card
- B132L+, B180L+:
  - One slot for a GSC (EISA formfactor) or PCI 32-bit/33 MHz, 5 V card
  - One slot for a GSC (EISA formfactor) or PCI 32-bit/33 MHz, 5 V or EISA card

Drives

- SCSI half-height 3.5âĂş 68-pin hard drive, either Fast-Wide high-voltage differential (on B132L, B160L) or Ultra-Wide SE (on **+**-models)
- 3.5âĂş Floppy drive
- SCSI half-heigth 5.25âĂş 50-pin SE drive, Fast-Narrow SE SCSI, externally accessible

3.18.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- *B132L, B160L* 68-pin HD SCSI-2 Fast-Wide *high-voltage differential*
- *B132L+, B180L+* SCSI-3 68-pin Ultra-Wide single-ended
- Two Serial RS232C DB9
- Parallel DB25
- *B132L, B160L* Ethernet RJ45
- *B132L+, B180L+* Fast Ethernet RJ45
- Ethernet AUI 15-pin
- EVC graphics port, that needs a special HP adapter cable to convert to VGA
- Two PS/2 connectors for keyboard & mouse
- Four phone jacks (microphone, headphones, line-in and line-out)

3.18.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- OpenBSD
- NetBSD

3.18.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95*rate*, int	SPEC95*rate*, fp
B132	6.45	6.70	58.1	60.3
B132+	6.84	7.17	61.5	64.6
B160L	7.75	7.56	69.7	68.1
B180L+	9.22	9.43	83.0	84.8

3.18.6 Dimensions

Height	Width	Depth	Weight
116mm	445mm	452mm	18kg

3.18.7 References

Manuals

- B-Class Owner's Guide (URL gone)
- B-Class Service Handbook (URL gone)

Articles

- A Low-Cost Workstation with Enhanced Performance and I/O Capabilities (.pdf) Scott P. Allan et al (June 1997: Hewlett-Packard Journal)

ROM update

There is an firmware update available for the B-Class, which contains the latest version 6.1

- PF_CB1X0061.txt has details about the contents and installation of the patch.
- CB1X0061.frm contains the patch.

3.19 HP Visualize B1000, C3000, C3600

3.19.1 Overview

These HP Visualize B-Class and C-Class PA-RISC workstations were aimed at the graphics workstations market, equipped with 64-bit PA-8500 processors featuring large on-chip L1 caches. Still part of the HP 9000 range of Unix PA-RISC workstations, they were sold in the late 1990s to early 2000s, and were some of the last PA-RISC desktop workstations.

The C3600 is essentially a C3000 upgraded to a PA-8600 CPU, the C3700 is the same, but upgraded to a PA-8700 CPU. There were additionally various more upgraded models, *e.g.*, the C3650 and the C3750, the former with a faster PA-8700 CPU, the latter with an even faster PA-8700+ CPU. The architecture was a major change from its predecessors with new I/O devices integrated and the LASI I/O chip removed together with the GSC bus. All device I/O is attached to PCI buses, external I/O devices are connected to USB ports.

Model numbers:

- B1000 and all C3x00/C3x50 have the 9000/785 model number

3.19.2 System

CPU

- B1000: PA-8500 300 MHz with 512/1024 KB on-chip I/D L1 cache
- C3000: PA-8500 400 MHz with 512/1024 KB on-chip I/D L1 cache
- C3600: PA-8600 552 MHz with 512/1024 KB on-chip I/D L1 cache
- C3650: PA-8700 625 MHz with 768/1536 KB on-chip I/D L1 cache
- C3700: PA-8700 750 MHz with 768/1536 KB on-chip I/D L1 cache
- C3750: PA-8700+ 875 MHz with 768/1536 KB on-chip I/D L1 cache

Chipset

- Astro memory/Runway controller
- Four Elroy PCI bridges
- National 87560 *(SuperI/O)*, handling USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C896 SCSI-3 controller

Buses

- Runway CPU/memory bus
- PCI-32/33 device I/O bus
- PCI-64/33 high-performance device I/O bus
- PCI-64/66 high-performance graphics I/O bus
- C37x0: PCI-64/100 high-performance graphics I/O bus
- SCSI-2 Ultra-Narrow single-ended external I/O bus
- SCSI-3 Ultra2-Wide LVD storage I/O bus
- IDE removable device I/O bus

Memory

- 278-pin 120 MHz ECC SDRAM DIMMs
- Eight slots for 128/256/512/1024 MB modules
- 128 MB to 8 GB supported

Expansion

- One PCI 64-bit/66 MHz, 3.3 V slot (clocked at 100 MHz on C37x0 systems)
- Three PCI 64-bit/33 MHz, 5 V slots
- Two PCI 32-bit/33 MHz, 5 V slots
- I/O slot layout (from top to bottom):
    1. PCI-64/33, pci0, 5 V
    2. PCI-64/66, pci1, 3.3 V (for primary graphics; on C37x0 systems this is a PCI-64/100 slot]
    3. PCI-64/33, pci0, 5 V
    4. PCI-64/33, pci2, 5 V (for secondary graphics)
    5. PCI-32/33, pci3, 5 V
    6. PCI-32/33, pci3, 5 V

Drives

- Two SCSI 3.5âĂş Ultra2-Wide LVD hard drives with 80-pin SCA connector
- 3.5âĂş Floppy drive
- Half-heigth IDE 5.25âĂş drive, external accessible

3.19.3 External

- SCSI-2 50-pin Ultra-Narrow single-ended
- SCSI-3 68-pin Ultra2-Wide LVD
- Two Serial RS232C DB9
- Parallel DB25
- Fast Ethernet RJ45
- Two USB ports for keyboard & mouse
- Four phone jacks (microphone, headphones, line-in and line-out)

3.19.4 Operating systems

- HP-UX: 10.20, 11.00 and 11i v1 (both only 64-bit releases)
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.19.5 Benchmarks

Model	**SPEC95, int**	**SPEC95, fp**	**SPEC95 *rate*, int**	**SPEC95 *rate*, fp**	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
B1000	23.9	39.3	217	378				
C3000	31.8	52.4	287	471	313	321		
C3600	42.0	64.0	379	576	432	433	5.0	5.0
C3650					508	542	5.9	6.3
C3700					604	576	7.0	6.7
C3750					678	674		

3.19.6 Dimensions

Model	**Height**	**Width**	**Depth**	**Weight**
Desktop	445mm	229mm	495mm	25kg
Rack-mounted	6U	451mm	665mm	25kg

3.19.7 References

Manuals

- B1000/C3x00 Owner's Guide (PDF, 4.9 MB)
- B1000/C3x00 Service Handbook (PDF, 3.2 MB)
- VISUALIZE Workstation Memory Subsystem (PDF, 120 KB)

3.20 HP Visualize B2000 and B2600

3.20.1 Overview

These HP Visualize B-Class PA-RISC workstations from 2000 were aimed at the graphics workstations market, equipped with the 64-bit PA-8500 or PA-8600 processors with large on-chip L1 caches. The B2000 usually uses the PA-8500 in a small tower case whereas the B2600 is built in a desktop, featuring the PA-8600 CPU. The architecture was a major change from those of its predecessors, the C200 et al, now based on Astro/Elroy, new I/O devices and without the LASI I/O chip and GSC bus. All device I/O now is implemented by PCI buses, human I/O devices are connected to USB ports.

Model numbers: both the B2000 and B2600 have the HP 9000/785 model number.

3.20.2 System

CPU

- B2000: PA-8500 400 MHz with 512/1024 KB on-chip I/D L1 cache
- B2600: PA-8600 500 MHz with 512/1024 KB on-chip I/D L1 cache

(there are some B2000s shipped with/upgraded to PA-8600 (PCXW+) processors)

Chipset

- Astro memory/Runway controller
- Two Elroy PCI bridges
- National 87560 (SuperI/O), handling USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip (on B2600 the audio card is optional)
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller
- B2000: Visualize FXe graphics

Buses

- Runway CPU/memory bus
- PCI-32/33 device I/O bus
- PCI-64/33 high-performance I/O bus
- SCSI-3 Ultra2-Wide LVD bus main storage I/O
- IDE bus; removable device-I/O

Memory

- 278-pin 120 MHz ECC SD-RAM DIMMs
- Four slots for 128 MB-1 GB modules
- 128 MB to 4 GB supported

Expansion

- Two PCI 64-bit/33 MHz, 5 V slots (clocked at 66 MHz on B2600)
- Two PCI 32-bit/33 MHz, 5 V slots
- B2000 I/O slot layout, from top to bottom:
  1. PCI-64/33, 5 V
  2. PCI-64/33, 5 V
  3. PCI-32/33, 5 V
  4. PCI-32/33, 5 V
- B2600 I/O slot layout, from top to bottom:
  1. PCI-32/33, 5 V, short PCI cards
  2. PCI-32/33, 5 V, short PCI cards
  3. PCI-64/33, 5 V, short and full-length cards
  4. PCI-64/33, 5 V, short and full-length cards

Drives

- Two SCSI 3.5âĂş Ultra2-Wide LVD hard drives with 80-pin SCA connector
- 3.5âĂş Floppy drive
- IDE half-heigth 5.25âĂş drive, external accessible

3.20.3 External

- B2000: VGA HD15
- Two Serial RS232C DB9
- Parallel DB25
- Fast Ethernet RJ45
- Two USB ports for keyboard & mouse
- Four audio jacks (microphone, headphones, line-in and line-out) (on B2600 the audio card is optional)

3.20.4 Operating systems

- HP-UX10.20 (unclear if B2600 supports 10.20), 11.00 and 11i v1
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.20.5 Benchmarks

Model	**SPEC95, int**	**SPEC95, fp**	**SPEC95 *rate*, int**	**SPEC95 *rate*, fp**	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
B2000	31.80	52.40	286	472	332	357	3.8	4.1
B2600					403	440	4.7	5.1

3.20.6 Dimensions

Model	**Height**	**Width**	**Depth**	**Weight**
B2000	445mm	229mm	495mm	21kg
B2600	127mm	425mm	457mm	20kg

3.20.7 References

Manuals

- B2000 Service Handbook (PDF, 8.8 MB)
- B2000 Owner's Guide (PDF, 2.6 MB)
- B2600 Technical Reference Manual (PDF, 33.0 MB)
- VISUALIZE Workstation Memory Subsystem (PDF, 120 KB)

3.21 HP 9000/C100 and C110

3.21.1 Overview

The HP 9000 C100 and C110 are PA-RISC graphics workstations based on the PA-7200 processor and were introduced in 1995. They have a similar case to that of the old HP 9000 735 — built of interlocking modules of the I/O and MPU board.

Model	Number	Introduced	Price
C100	9000/777	1995	$19,715
C110	9000/777	1995	$25,715

3.21.2 System

CPU

- C100: PA-7200 100 MHz with 256/256 KB off-chip I/D L1 cache and 2 KB on-chip "assist" L1 cache
- C110: PA-7200 120 MHz with 256/256 KB off-chip I/D L1 cache and 2 KB on-chip "assist" L1 cache

Chipset

- U2 I/O adapter Runway to GSC bridge
- MMC/SMC memory controllers
- LASI I/O chipset
- NCR 53C710 8-bit single-ended SCSI-2
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Wax EISA bridge
- GSC graphics
- Other I/O (serial, parallel, HP-HIL, Floppy)

Buses

- Runway CPU/memory bus (100 MHz 800 MB/s peak data rate on C100, 120 MHz, 960 MB/s on C110)
- GSC general system-level I/O bus
- EISA additional expansion I/O bus
- SCSI-2 single-ended bus

- SCSI-2 Fast-Wide *high-voltage differential* main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- 400 MB/s (C100), 480 MB/s (C110) peak bandwidth
- Eight slots for 16-128 MB modules
- 32 MB to 1 GB supported

Expansion

- One slot for a GSC (EISA formfactor) card
- Three slots for GSC (EISA formfactor) or EISA cards
- I/O slot layout (from top to bottom):
  1. EISA or GSC
  2. EISA or GSC
  3. EISA or GSC (for secondary graphics)
  4. GSC (for primary graphics)

Drives

The disk slider can accomodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25âĂş CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5âĂş 68-pin Fast-Wide *high-voltage differential* system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Fast-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- Two 3.5âĂş 68-pin Fast-Wide differential (HVD) SCSI hard drives,
- One 3.5âĂş Floppy drive and
- One external-accessible half-height 5.25âĂş SCSI drive (CD/DAT).

3.21.3 External

- SCSI-2 50-pin single-ended
- SCSI-3 68-pin Fast-Wide *differential* (HVD)
- Two Serial RS232C DB9 (up 460.8Kb/s)
- Parallel DB25
- Ethernet RJ45
- Ethernet AUI 15-pin
- Graphics port depend on installed video adapter
- Two PS/2 connectors for keyboard and mouse
- HP-HIL for input device loop
- Four phone jacks (microphone, headphones, line-in and ?)

3.21.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.21.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
C100	4.98	6.59	44.8	59.4
C110	6.00	8.14	54.0	73.3

3.21.6 Dimensions

Height	Width	Depth	Weight
138mm	539mm	447mm	21kg

3.21.7 References

Manuals

- C100/110 Owners Guide (PDF, 1.6 MB)
- Service Handbook C Class (PDF, 1.5 MB)

3.22 HP Visualize C132L, C160L

3.22.1 Overview

The HP Visualize C132L and C160L PA-RISC workstations were entry-level Unix workstations with integrated, low-cost PA-7300LC processors and LASI chipset. They have a similar case to that of the old HP 9000/735 workstation — built of interlocking modules so the I/O board, MPU board etc. can be easily taken out.

The C132L and C160L were close to the slightly older and less powerful C100/C110, which were PA-7200 based, and technically almost identical to the smaller and less expandable B132L/B160L workstations.

The very rare PA-RISC laptops from RDI, the RDI PrecisionBooks from 1998, were technically based on the Visualize C132L, C160L and C180L.

Model	Number	Introduced	Price
C132L	9000/779	1996	
C160L	9000/779	1996	$19,480

3.22.2 System

CPU

- C132L: PA-7300LC 132 MHz with 128 KB on-chip L1 and 1 MB off-chip L2 cache
- C160L: PA-7300LC 160 MHz with 128 KB on-chip L1 and 1 MB off-chip L2 cache

The off-chip L2 cache SRAM is optional and installed in two DIMM slots below the CPU socket, usually two 512 KB modules for 1 MB L2 cache.

Chipset

- LASI chipset
- Phantom PseudoBC GSC+ port
- NCR 53C710 8-bit single-ended SCSI-2
- NCR 53C720 16-bit Fast-Wide *differential* (HVD) SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Wax EISA bridge
- Dino GSC-to-PCI bridge
- Visualize-EG graphics with 2MB frame buffer memory
- Other I/O (serial, parallel, Floppy, HP-HIL)

Buses

- GSC-2 system and I/O bus (33 MHz with 132 MB/s peak data rate on C132L, 40 MHz 160 MB/s on C160L)
- EISA additional expansion I/O bus
- PCI-32/33 high-performance device I/O bus
- SCSI-2 single-ended bus
- SCSI-2 Fast-Wide *differential* main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- 12 slots for 16-256 MB modules
- 32 MB to 2 GB supported

Expansion

- Two slots for GSC (EISA formfactor) or EISA cards
- One slot for a PCI 32-bit/33 MHz, 3V or EISA card
- One slot for a PCI 32-bit/33 MHz, 3V card
- Slot layout, from top to bottom:
    1. EISA or GSC
    2. EISA or GSC
    3. PCI-32/33.3 V or EISA
    4. PCI-32/33

Drives

The disk-slider can accomodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25âĂş CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5âĂş 68-pin Fast-Wide *high-voltage differential* system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Fast-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- Two 3.5âĂş 68-pin Fast-Wide differential (HVD) SCSI hard drives,
- One 3.5âĂş Floppy drive and
- One external-accessible half-height 5.25âĂş SCSI drive (CD/DAT).

3.22.3 External

- SCSI-2 50-pin single-ended
- SCSI-3 68-pin Fast-Wide *differential* (HVD)
- Two Serial RS232C DB9 (up 460.8Kb/s)
- Parallel DB25
- Ethernet RJ45
- Ethernet AUI 15-pin
- EVC graphics port, that needs a special HP adapter cable to convert to VGA
- Two PS/2 connectors for keyboard and mouse
- HP-HIL for input device loop
- Four phone jacks (microphone, headphones, line-in and ?)

3.22.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- OpenBSD
- NetBSD

3.22.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95*rate*, int	SPEC95*rate*, fp
C132L	6.45	6.70	58.1	60.3
C160L	7.75	7.56	7.75/7.56	69.7/68.1

3.22.6 Dimensions

Height	Width	Depth	Weight
138mm	539mm	447mm	21kg

3.22.7 References

Manuals

- C160L Owners Guide (PDF, 1.6 MB)
- Service Handbook C Class (PDF, 1.5 MB)

3.23 HP Visualize C160, C180

3.23.1 Overview

The HP Visualize C160 and C180 workstations were graphics workstations equipped with 64-bit PA-8000 processors, introduced in 1996. The C160 and C180 were higher-end offerings with faster CPUs and better configurations compared to older HP Visualize C100, C110, or lower-cost C132L, C160L. The case is similar to that of the HP 9000/735 workstation, built of interlocking modules. These machines were aimed at CAD/CAM/3D modelling.

The C180 is also sometimes referred to as **C180XP**

Model numbers: both the C160 and C180 have the HP 9000/780 model number.

3.23.2 System

CPU

- C160: PA-8000 160 MHz with 512/512 KB off-chip I/D L1 cache
- C180: PA-8000 180 MHz with 1024/1024 KB off-chip I/D L1 cache

Chipset

- UTurn I/O adapter Runway to GSC bridge
- MMC/SMC memory controllers
- LASI I/O chipset
- NCR 53C710 8-bit single-ended SCSI-2
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Wax EISA bridge
- Dino GSC-to-PCI bridge
- Visualize-EG graphics with 2MB frame buffer memory
- Other I/O (serial, parallel, Floppy, HP-HIL)

Buses

- Runway CPU/memory bus (120 MHz with 960 MB/s peak bandwidth)
- Cache: 128-bit wide bus between cache and CPU
  - C160: 2.56 GB/s I-fetch, 2.56 GB/s D-load (16-Byte), 1.26 GB/s D-store (8-Byte)
  - C180: 2.88 GB/s I-fetch, 2.88 GB/s D-load (16-Byte), 1.44 GB/s D-store (8-Byte)

- GSC-2 general system-level I/O bus
- EISA additional expansion I/O bus
- PCI-32/33 high-performance device I/O bus
- SCSI-2 single-ended bus
- SCSI-2 Fast-Wide *high-voltage differential* main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- 960 MB/s peak bandwidth
- 12 slots for 16-256 MB modules
- 32 MB to 3 GB supported

Expansion

- One slot for a GSC (EISA formfactor) or PCI 32-bit/33 MHz, 3.3 V card
- One slot for a GSC (EISA formfactor), EISA or PCI 32-bit/33 MHz, 3.3 V card
- Two slots for GSC (EISA formfactor) or EISA cards
- I/O slot layout, from top to bottom:
  1. EISA or GSC
  2. EISA or GSC
  3. PCI-32/33, 3.3 V or EISA or GSC
  4. PCI-32/33, 3.3 V or GSC

Drives

The disk-slider can accomodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25âĂş CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5âĂş 68-pin Fast-Wide *high-voltage differential* system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Fast-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- Two 3.5âĂş 68-pin Fast-Wide differential (HVD) SCSI hard drives,
- One 3.5âĂş Floppy drive and
- One external-accessible half-height 5.25âĂş SCSI drive (CD/DAT).

3.23.3 External

- SCSI-2 50-pin single-ended
- SCSI-3 68-pin Fast-Wide *differential* (HVD)
- Two Serial RS232C DB9 (up 460.8Kb/s)
- Parallel DB25
- Ethernet RJ45
- Ethernet AUI 15-pin
- EVC graphics port, that needs a special HP adapter cable to convert to VGA
- Two PS/2 connectors for keyboard and mouse
- HP-HIL for input device loop
- Four phone jacks (microphone, headphones, line-in and ?)

3.23.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.23.5 Benchmarks

Model	**SPEC95, int**	**SPEC95, fp**	**SPEC95*rate*, int**	**SPEC95*rate*, fp**
C160	10.40	16.30	93.6	147
C180	11.80	18.70	107	169

3.23.6 Dimensions

Height	**Width**	**Depth**	**Weight**
138mm	539mm	447mm	21kg

3.23.7 References

Manuals

- Model C160 / C180 / C200 / C240 / C360 Owner's Guide (PDF, 1.5 MB)
- Service Handbook C Class (PDF, 1.5 MB)

ROM update

There is a firmware update available for the C160 and C180, which contains the latest version (*6.2*).

- PF_CC2X0062.text has details about the contents and installation of the patch.
- PF_CC2X0062.frm contains the patch.

3.24 HP Visualize C200, C240, C360

3.24.1 Overview

The HP Visualize C200, C240 and C360 PA-RISC workstations were aimed at the late-1990s Unix graphics market, with powerful 64-bit PA-8200 and PA-8500 CPUs. They have a similar case to that of the old 735 — built of interlocking modules so the I/O board, MPU board etc. can be easily taken out. These machines were aimed at CAD/CAM/3D modelling, and were at the time the fastest configurations of the C-Class series.

The systems were sometimes referred to as C200**+** and C240**+**, as well as by their previous HP 9000 prefix.

Model	Number	Introduced	Price
C200	9000/782	1997	$21,000
C240	9000/782	1997	$46,000
C360	9000/785	1998	$22,365

Note that list prices were moving in 97-98 a lot due to pressure from Windows NT workstations and HP adjusting prices often in response.

3.24.2 System

CPU

- C200: PA-8200 200 MHz with 512/1024 KB off-chip I/D L1 cache
- C240: PA-8200 236 MHz with 2048/2048 KB off-chip I/D L1 cache
- C360: PA-8500 367 MHz with 512/1024 KB on-chip I/D L1 cache

Chipset

- UTurn I/O adapter Runway to GSC bridge
- MMC/SMC memory controllers
- LASI I/O chipset
- NCR 53C710 8-bit single-ended SCSI-2
- Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- Intel 82596CA 10 Mbit Ethernet controller
- DEC 21142/43 *(Tulip)* Fast-Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Wax EISA bridge
- Dino GSC-to-PCI bridge
- Cujo GSC-to-PCI bridge, 64-bit

- Other I/O (serial, parallel, Floppy)

Buses

- Runway CPU/memory bus (120 MHz with 960 MB/s peak data rate)
- GSC-2 general system-level I/O bus (256 MB/s)
- EISA (built to order option), additional expansion I/O
- PCI-32/33 device I/O bus
- PCI-64/66 high-performance device I/O bus
- SCSI-2 Fast-Narrow single-ended bus
- SCSI-2 Ultra-Wide single-ended bus main storage I/O

Memory

- 72-pin ECC EDO SIMMs, 50ns or faster
- 12 slots for 16-256 MB modules
- 32 MB to 3 GB supported

Expansion

- Three slots for GSC (EISA formfactor) or PCI cards
- One slot for a GSC (EISA formfactor), PCI or EISA card
- Two of the PCI slots are PCI 32-bit/33 MHz, 5 V; the other two PCI 64-bit/66 MHz, 3.3 V. Some system do not have the optional EISA slot
- I/O slot layout, from top to bottom:
  1. PCI-32/33, 5 V or EISA or GSC
  2. PCI-64/66, 3.3 V or GSC
  3. PCI-32/33, 5 V or GSC
  4. PCI-64/66, 3.3 V or GSC

Drives

The disk-slider can accomodate up to three SCSI drives and one floppy drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a SE-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25âĂș CD/DAT drive, although it is of course also possible to connect a 50-pin SE hard drive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE hard drives. The PDC can boot off these SE drives.

The *Wide-SCSI* cable is normally used for the internal 3.5âĂș 68-pin Ultra-Wide SE system drives. Up to three hard drives can be installed in the cage, which leaves no room for an external-accessible CD/DAT drive though. The Ultra-Wide drives are also bootable from the PDC.

A standard configuration could look like this:

- Two 3.5âĂș 68-pin Ultra-Wide single-ended (SE) SCSI hard drives,
- One 3.5âĂș Floppy drive and
- One external-accessible half-height 5.25âĂș SCSI drive (CD/DAT).

3.24.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- SCSI-3 68-pin Ultra-Wide single-ended
- Two Serial RS232C DB9
- Parallel DB25
- Fast Ethernet RJ45
- Ethernet AUI 15-pin
- Two PS/2 connectors for keyboard & mouse
- Four phone jacks (microphone, headphones, line-in and ?)

3.24.4 Operating systems

- HP-UX10.20, 11.00 and 11iv1
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.24.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
C200	14.20	21.40	129	193
C240	17.10	25.40	156	229
C360	26.00	28.10	234	252

3.24.6 Dimensions

Height	Width	Depth	Weight
138mm	539mm	447mm	23kg

3.24.7 References

Manuals

- Model C160 / C180 / C200 / C240 / C360 Owner's Guide (PDF, 1.5 MB)
- Service Handbook C Class (PDF, 1.5 MB)

Other

- HP C200/C240/C360 Power Supply problems - solved USENET posting

3.25 HP C8000

3.25.1 Overview

The HP C8000 is the last PA-RISC HP workstation, powered by one or two dual-core PA-8800 *Mako* processors, later offered with PA-8900 CPUs and features an impressive array of system and I/O options. The center of the system is the HP *zx1* chipset, which also supports Itanium processors. The system is built in a sleek, silent tower casing and also available as a rack-mount option.

3.25.2 System

CPU

- 1-2 PA-8800 (dual-core) 900 MHz-1.0 GHz with 1.5 MB/1.5 MB on-chip I/D L1 cache and 32 MB off-chip L2 cache each
  or
- 1-2 PA-8900 (dual-core) 800 MHz-1.1 GHz with 1.5 MB/1.5 MB on-chip I/D L1 cache and 64 MB off-chip L2 cache each

Chipset

- HP **zx1** chipset
  - Pluto zx1 MIO (memory and I/O controller) connects to the processor bus (6.4 GB/s), two memory buses (each 4.25 GB/s) and seven I/O channels (aggregate 3.5 GB/s) and contains both memory and cache controllers
  - Six Mercury zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 3.5 GB/s on seven 0.5 GB/s channels
    1. AGP 4x graphics bus on two channels — 1.0 GB/s
    2. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
    3. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
    4. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
    5. Gigabit Ethernet and Ultra320 SCSI on PCI 64/66 on one channel — 0.5 GB/s
    6. IDE, USB, management LAN on PCI 32/33 on one channel — 0.5 GB/s
- Gigabit Ethernet controller
- Two-channel Ultra-320 SCSI controller
- UltraATA-133 IDE controller
- 8 MB Flash EEPROM

Buses

- Itanium 2/zx1 processor bus 6.4 GB/s
- Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s — aggregate 8.5 GB/s memory bandwidth
- Seven zx1 I/O channels/buses, aggregate 3.5 GB/s
- AGP 8x graphics bus
- PCI-X 64/133 I/O bus
- PCI-X 64/66 I/O bus
- PCI 64/33 I/O bus
- PCI 32/33 I/O bus
- SCSI-3 Ultra320 (LVD) storage I/O bus
- UltraATA-133 IDE secondary storage I/O bus

Memory

- PC2100 registered ECC DDR266 SDRAM DIMMs
- Takes up to 4 GB modules
- Eight slots
- 32 GB maximum
- 8.5 GB/s memory bandwidth
- 80ns memory latency

Expansion

- One PCI-X 64-bit/133 MHz slot, full-length
- Two PCI-X 64-bit/66 MHz slots, full-length
- One PCI 64-bit/33 MHz slot, full-length
- Two PCI 32-bit/33 MHz slots, half-length
- All PCI slots are 3.3 V
- One AGP Pro 8x slot (150W max power with auxiliary power connector)
- I/O slot layout (from top to bottom):
    1. PCI-32/33, short PCI cards
    2. PCI-32/33, short PCI cards
    3. AGP-8X pro
    4. PCI-64/33, short and full-length cards

5. PCI-64/66, short and full-length cards
6. PCI-64/66, short and full-length cards
7. PCI-64/133, short and full-length cards

Drives

- Up to four internal 3.5âĂș bays for Ultra320 LVD SCSI hard drives with 68-pin connector
- Up to two internal 3.5âĂș bays for UltraATA-133 IDE hard drives
- Three half-heigth 5.25âĂș bays for externally accessible SCSI (LVD or SE) or UltraATA-133 drives

3.25.3 External

- Two Serial RS232C DB9
- Five USB 2.0 ports (two in front, three in rear)
- TP/RJ45 Gigabit Ethernet
- Four phone jacks (microphone, headphones, line-in and line-out) on optional 16-bit audio card

3.25.4 Operating systems

- HP-UX: 11i v1
- Linux

3.25.5 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000*rate*, int	SPEC2000*rate*, fp
C8000		1001 (est.)		

3.25.6 Dimensions

Model	Height	Width	Depth	Weight
	490mm	287mm	572mm	21kg
Rack-mounted	5U	424mm	572mm	21kg

3.25.7 References

Manuals

- HP Workstation c8000 Technical Reference Guide (PDF, 2.7 MB, kernel.org mirror)
- QuickSpecs HP c8000 Workstation (PDF, 400 KB)

3.26 HP 9000/D-Class and R-Class

3.26.1 Overview

The HP 9000 D-Class servers were flexible, upgradable and scalable PA-RISC enterprise servers for Unix applications from the mid- to late-1990s. They were designated to bring "mid-range performance for an entry-level price," with processors from 32-bit PA-7100LC to 64-bit PA-8200 and some multi-processing SMP support. All D-Class servers were members of the HP 9000 800 server series and used two main different architectures: LASI for PA-7100LC/PA-7300LC models and U2/UTurn for PA-7200/PA-8000 models.

In the 1990s, D-Class servers were part of the US Navy TAC-4 program, in which HP was a vendor supplying RISC Unix computers for uses throughout the Navy. The D-Class were part of a technology refreshment of TAC-4 in 1996.

R-Class "Ultralight" servers R380 and R390 are rack-mountable versions of their D-Class counterparts D380/D390. They are technically almost identical, except some differences in the I/O and storage configuration.

Different models were available which could be upgraded within the series to another model with various options for each system. The servers used the following naming convention and were part of the HP 9000 800 series:

- The first number after the "D", **2** or **3**, indicates the general D-Class type — the D**2**x0 were smaller servers, the D**3**x0 bigger with more expansion and options.
- Ending numbers **00, 10, âĂę 90** indicate the system and features like CPU and chipset.
- **R**380/**R**390 are R-Class rack-mountable servers for 19" racks.

System	Model number	Introduced	Price
D200, D300	HP 9000/801	January 1996	
D210, D310	HP 9000/811	January 1996	$6,900
D220, D320	HP 9000/803, HP 9000/813	January 1997	$8,900
D230, D330	HP 9000/823, HP 9000/833	January 1997	$16,700
D250, D350	HP 9000/821, HP 9000/831	January 1996	
D260, D360	HP 9000/841, HP 9000/851	May 1996	
D270, D370	HP 9000/861, HP 9000/871	November 1996	
D280, D380	HP 9000/810, HP 9000/820	September 1997	
D390	HP 9000/800	July 1998	
R380, R390	HP 9000/800	September 1998	

3.26.2 System

CPU

- D200/D300: PA-7100LC 75 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- D210/D310: PA-7100LC 100 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- D220/D320: PA-7300LC 132 MHz with 128 KB on-chip L1 (and 1 MB off-chip L2) cache
- D230/D330: PA-7300LC 160 MHz with 128 KB on-chip L1 (and 1 MB off-chip L2) cache

- D250/D350: 1-2 PA-7200 100 MHz with 512 KB off-chip L1 and 2 KB on-chip L1 cache each
- D260/D360: 1-2 PA-7200 120 MHz with 2 MB off-chip L1 and 2 KB on-chip L1 cache each
- D270/D370: 1-2 PA-8000 160 MHz with 1 MB off-chip L1 cache each
- D280/D380/R380: 1-2 PA-8000 180 MHz with 2 MB off-chip L1 cache each
- D390/R390: 1-2 PA-8200 240 MHz with 4 MB off-chip L1 cache each

Notes

- Systems with PA-7100LC/PA-7300LC processors are only single-CPU
- Systems with PA-7300LC processors have optional 1 MB external L2 cache on two SRAM modules

Chipset

- *PA-7200 models* U2 I/O adapter Runway to GSC bridge
- *PA-8000 models* UTurn I/O adapter Runway to GSC bridge
- *PA-7200/PA-8000 models* MMC/SMC memory controllers
- *PA-7300LC models* Phantom PseudoBC GSC+ port
- LASI I/O chipset
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit audio
- Wax EISA bridge
- *D3x0* NCR 53C720 16-bit Fast-Wide high-voltage differential (HVD) SCSI-2
- *D390/R380/R390* DEC 21140 Fast Ethernet controller
- Other I/O (serial, parallel)

Buses

- On SMP-capable systems: Runway CPU/memory bus
- GSC+ bus for the general system level I/O
- EISA expansion bus
- *D3x0* SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage I/O
- SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Note: the Fast-Wide differential bus is optional on the D2x0 models.

Memory

- 72-pin ECC SIMMs

Systems with a PA-8x00 need 50ns access time modules, PA-7200 and PA-7300LC models can take up to 60ns, PA-7100LC even slower modules.

Expansion

- D2x0:
  - One slot for a GSC/HSC card in EISA formfactor
  - Two slots for EISA cards
  - Three slots for either GSC/HSC in EISA formfactor or EISA cards
- D3x0:
  - One slot for a GSC/HSC card in EISA formfactor
  - Three slot for EISA cards
  - Four slots for either GSC/HSC in EISA formfactor or EISA cards
- R380/R390:
  - One slot for a GSC/HSC card in EISA formfactor
  - Four slot for EISA cards
  - Three slots for either GSC/HSC in EISA formfactor or EISA cards

Drives

- *D-Class* Up to three 5.25âĂş 50-pin Fast-Narrow SE SCSI half-height drives, external accessible
- *D2x0/R3x0* Up to two Fast-Narrow 50-pin SCSI-2 single-ended hard drives
- *D3x0* Five hot-swap trays for a Fast-Wide 68-pin SCSI-2 high-voltage differential hard drive
- *R3x0* One 5.25âĂş 50-pin Fast-Narrow SE SCSI half-height drive, external accessible
- With the Fast-Wide differential SCSI option on D2x0 two optional trays for FWD drives are available.

3.26.3 External

- SCSI-2 50-pin single-ended
- TP/RJ45 10BaseT 10 Mbit Ethernet
- Two Serial RS232C DB9, one for console, one for USV
- Parallel DB25
- Two PS/2 connectors for keyboard und mouse

3.26.4 Operating systems

- HP-UX 10.20 for 800s servers, HP-UX 11.00 and 11i v1
- Linux
- OpenBSD: D220, D230, D320, D330
- NetBSD: D200, D210, D220, D230, D300, D310, D320, D330

3.26.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp	SPEC95*rate*, int	SPEC95*rate*, fp
Dx00	115	146	2.18	2.90	19.2	25.8
Dx10	152	194	3.74	4.08	33.6	36.7
Dx20			6.57	6.72	59.2	60.5
Dx30			7.87	7.58	70.8	68.3
Dx50	144	218	5.01	6.77	45.1	61.0
Dx60						
Dx60					114	143
Dx70			10.40	15.00	93.9	135
Dx702-CPU					184	190
Dx80			12.30	17.40	111	157
Dx802-CPU					219	221
D390			15.50	25.50		

3.26.6 References:

Manuals

- D-Class and R-Class Installation Guide (URL gone)
- D-Class and R-Class Operator's Guide (URL gone)
- D-Class and R-Class System Upgrade Guide (URL gone)

Articles

- An Entry-Level Server with Multiple Performance Points (.pdf) Lin A. Nease et al (June 1997: Hewlett-Packard Journal)

3.27 HP 9000/E-Class

3.27.1 Overview

The E-Class "Wright Brothers" are low-cost PA-RISC servers from the mid-1990s and replacements for the older F and G-Class Nova servers. Designed for reduced manufacturing cost they were developed in parallel to the HP 9000/712 workstations. The case was taken over almost unchanged from the F-Class, with the CPU/memory and part of the I/O systems being new designs. From the integrated LASI chipset only the networking and several other functions were used — due to time constraints a modified version of the F-Class HP-PB "Personality boards" was used for SCSI, serial MUX and parallel.

Model numbers, introductions dates and prices:

System	Model number	Introduced	Price
E25	HP 9000/806	1994	$6,000
E35	HP 9000/816	1994	
E45	HP 9000/826	1994	$11,320
E55	HP 9000/856	1995?	

3.27.2 System

CPU

- E25: PA-7100LC 48 MHz with 1 KB on-chip L1 and 64 KB off-chip L1 cache
- E35: PA-7100LC 64 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- E45: PA-7100LC 80 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache
- E55: PA-7100LC 96 MHz with 1 KB on-chip L1 and 1024 KB off-chip L1 cache

Chipset

- LASI as central I/O chipset
- Wax EISA bridge
- HP-PB bus converter, 8 MHz HP-PB frequency
- HP ASICs for HP-PB, SCSI and MUX port

Buses

- GSC system level I/O bus
- HP-PB additional I/O bus
- SCSI-2 Fast-Narrow single-ended bus; main storage I/O

Memory

- 72-pin ECC SIMMs, 8-64 MB modules
- Eight slots
- 16 MB minimum, 512 MB maximum

Expansion

- Two slots for HP-PB cards

Drives

- One tray for two 3.5âĂş Fast-Narrow SE 50-pin SCSI hard drives
- One tray for three half-height 5.25âĂş Fast-Narrow SE 50-pin drives, externally accessible

3.27.3 External

- SCSI-2 50-pin single-ended
- high-pin-count MUX connector
- Ethernet RJ45
- Ethernet AUI 15-pin
- Parallel DB25

3.27.4 Operating systems

- HP-UX 10.20 for 800s servers, HP-UX 11.00 and HP-UX 11i v1 (unsupported)
- Linux: very limited hardware support (no SCSI and other)
- NetBSD: very limited hardware support (no SCSI, only serial and other)

3.27.5 Benchmarks

Model	SPEC92, int	SPEC92, fp
E25	45.0	66.7
E35	65.6	98.5
E45	82.1	122.9
E55	108.0	163.4

3.27.6 References

- Development of a Low-Cost, High-Performance, Multiuser Business Server System (PDF, HP Journal 4/95)

◈ HP 9000 E-Class Servers Product Brief (.pdf) Hewlett-Packard Company (1993: Hewlett-Packard)

3.28 HP 9000 500 FOCUS

3.28.1 Overview

With Frank McConnell; some parts taken with permission from him.

The HP 9000/500s computers were the early-1980s predecessors of the PA-RISC workstations and the first member of the HP 9000 series. Although already based on a HP 32-bit processor — the FOCUS — they did not have PA-RISC CPUs yet, which were developed only later.

The HP 9000/520, originally 9020, the first HP 9000 series, was introduced in 1982 by HP and one year later described in the Hewlett Packard Journal as "the new HP 9000 computer, a mainframe on the desktop." All 500s used the same HP FOCUS processor, memory and I/O; differences were in casing, expandability and built-in I/O.

The HP 9000/500 series was phased out in the late 1980s, probably due to the complexity and cost of its architecture and was replaced by HP PA-RISC (700/800 series) and M68K (300/400 series) running HP-UX. The first PA-RISC NMOS implementation had one third the amount of FETs of the FOCUS processor and was a much more streamlined design.

Table 3.64: HP 9000/520, 530, 540 and 550 introduction dates and prices

Model	Introduced	Price
520	1982	$30,000
530	1982	$23,105
540	1982	$24,115
550	1984	

The HP 9000 520 was used widely by the US Navy from the mid-1980s under the DTC program as a desktop computer for a variety of tactical uses. Originally called Desk-Top Computer (DTC) in 1982, later becoming Desktop Tactical Computer (DTC-1), the program looked at using commercial COTS desktop computers for tactical decision support in US Navy facilities and ships. After evaluation throughout the Navy, the contract was awarded to HP, after which the 9020C version (520 workstation with 13" monitor) became widely deployed throughout the Navy.

About the Joint Operational Tactical System, JTOS, of which the 9020C was an integral part, from the HP Computer Museum (Bill Reed article):

> "Despite the fact that some naval leaders didn't see the point of JOTS, at one time, almost every tactical or fleet staff in the United States Navy had five or more HP 9000s, often networked together. Some had the early projection systems for common displays. There was a sharing of the load, so to speak. The computers gave those that processed anti-submarine warfare what they wanted on one terminal while those involved with anti-air warfare processed on another computer. The technology that ensued included special interface boards capturing radar systems, communications systems and aircraft systems, many connected with fiber optics."

3.28.2 Systems

Four distinct models were introduced between 1982 and 1984, based on the same architecture:

HP 9000/520 *Dawn*, also called HP 9020

- ◈ Original desktop version, Introduced 1982 for $30,000
- ◈ 1-3 HP FOCUS processors, 18 MHz
- ◈ 16 KB cache
- ◈ 512 KB RAM to 10 MB maximum
- ◈ One IOP, with up to three supported
- ◈ 5.25″ floppy, optional 10 MB hard drive
- ◈ 9020A: 12″ color monitor with 512×390 resolution
- ◈ 9020B: 12″ monochrome (green) monitor with 560×455 resolution
- ◈ 9020C: 13″ color monitor with 560×455 resolution
- ◈ 9020AS (bundled system): 9020A with 1 MB RAM, the optional 10 MB hard drive, thermal printer, HP BASIC operating system
- ◈ 9020AT (bundled system): 9020A with 1.5 MB RAM, thermal printer, HP-UX operating system (single-user)

HP 9000/530 *Corona*, also called HP 9030:

- ◈ 19″ rack-mount version, introduced 1982 for $23,105
- ◈ 1-3 HP FOCUS processors, 18 MHz
- ◈ 16 KB cache
- ◈ 512 KB RAM to 10 MB maximum
- ◈ One IOP, with up to three supported
- ◈ 9030A: base system (probably equals 9030)

HP 9000/540 *Corona*, also called HP 9040:

- ◈ Free-standing cabinet system, introduced 1982 for $24,115
- ◈ 1-3 HP FOCUS processors, 18 MHz
- ◈ 16 KB cache
- ◈ 512 KB RAM to 10 MB maximum
- ◈ 9040A: base system (probably equals 9040)
- ◈ 9040AT (bundled system): 9040A with 1.5 MB RAM, HP-UX operating system (single-user)
- ◈ 9040AM (bundled system): 9040A with 1.5 MB RAM, HP-UX operating system (multi-user)

HP 9000/550 *Shuttle*, also called HP 9050:

- ◈ Industrial system that replaced 530 and 540, introduced in 1984
- ◈ 1-3 HP FOCUS processors, 18 MHz
- ◈ 16 KB cache
- ◈ 512 KB RAM to 10 MB maximum
- ◈ Up two four Display Station Buffer Cards (DSBs) graphics adapters

- ◈ HP-IB interface ("medium-speed")
- ◈ 9050A: base system (probably equals 9050)
- ◈ 9050AT (bundled system): 9050A with 1.5 MB RAM, HP-UX operating system (single-user)
- ◈ 9050AM (bundled system): 9050A with 1.5 MB RAM, HP-UX operating system (multi-user)

HP 9000/500s in SMP configuration were also called *600 series* (some of the 1980s' 800s server systems were also called 600 series for a short time).

Possible I/O and expansion options for the 500s:

- ◈ HP-IB card for external HP-IB (HP Instrumentation Bus) devices
- ◈ GP-IO card for GP-IO (General Purpose I/O) devices with 8-bit or 16-bit DMA
- ◈ Asynchronous Serial
- ◈ I/O Expander for eight I/O channels/slots (CIO) for additional IOPs
- ◈ LAN 9000, 10 Mbit Ethernet (coax)

3.28.3 Processors

The basic architecture of the 500 series was Hewlett-Packard FOCUS, implemented in five NMOS-III VLSI chips fabbed in 1.5 micron: the CPU chip, I/O processor (IOP), memory controller, 128Kb RAM (16 KB cache) and clock driver.

The CPU ran at 18 MHz and had a "direct address range" of "500 MB" (probably 29-bit direct addressing for 512 MB). It was fabricated with 450,000 FETs, integrated with three Floating-Point chips onto one "finstrate" CPU board. The FOCUS CPU was microcoded with 9,000 38-bit microcode control stores and implemented the HP 3000 computers' stack-based architecture in 32-bit. All internal data paths and registers are 32-bit wide. Due to heat dissipation difficulties the ICs were mounted on special printed-circuit boards called "finstrates" — the board has a 1mm copper sheet as core to which the IC substrate is epoxied directly.

The I/O Processor IOP executes all I/O instructions and handles the transactions from/to the eight attached HP CIO channels. It has an I/O bandwith of 5.1 MB/s burst and 973 KB/s multiplexed. The IOP was also a microprogrammed (4,608 32-bit microcode stores) NMOS-III VLSI chip.

At least one IOP to interface with the I/O buses was needed so up to six CPUs were supported in hardware but only three in software. Up to two additional IOPs could be installed for more I/O options; each additional IOP needed an I/O expander which provided the I/O channels extension, the CIO bus.

The three finstrates boards of CPU, IOP and 256 KB RAM were installed in a 12-slot HP 9000/520 module. This allowed configurations of up to 10 MB of RAM; memory cards could be substituted to construct multiprocessor systems. The CPU, IOP and memory controller communicated via the memory processor bus **MPB**. The 44-line, 18 MHz, 36 MB/s MPB supports up to seven (other sources mention three/three) CPUs or IOPs and fifteen memory controllers.

3.28.4 Architecture

The FOCUS is a stack architecture, with 230 instructions (both 32 bits and 16 bits wide), a segmented memory model, and no general purpose programmer-visible registers. There are thirty-nine 32-bit

registers in the CPU hardware — thirty-one internal 32-bit general purpose registers, two 32-bit ALU registers, and others.

It has a flat address space but that is not really what most programs see: their access to memory is largely described by registers that contain the absolute memory addresses of segment boundaries. For example, instructions come from the current code segment, which is described by three registers: **P**, the program counter, which is a 32-bit register containing the absolute address of the instruction being executed; **PB**, the program base register, which is a 32-bit register containing the absolute address of the first word of the current code segment; and **PL**, the program limit register, which is a 32-bit register containing the absolute address of the last word of the current code segment.

The data segment also has base (**DB**) and limit (**DL**) registers, and so does the stack segment (**SB, SL**). The stack segment also has a stack pointer (**S**) and a stack marker pointer (**Q**) which points to the current procedure's activation record on the stack.

There is also an index register, a status register, a flags register (really a sort of debugging-state register), a message register (interrupting conditions) and message mask register (which enables/disables interrupts from the message register), a breakpoint register, and a couple of registers which are for the memory controllers to talk to the CPU.

The machine instruction set is oriented toward moving words between memory and the top of the stack, and operating on the words at the top of the stack. To take an addition of two numbers: load one, load the other, execute an **ADD** instruction, and then a store instruction if the result should be kept somewhere in memory other than on the stack.

The stack is in memory, there are (probably) some numbers of "top of stack" registers inside the processor to keep things moving relatively quickly, but these registers are not otherwise visible to the programmer.

3.28.5 Software

A choice of operating systems was provided by HP for the 520: HP BASIC or HP-UX. The 530, 540 and 550 only supported HP-UX. HP-UX ran until version 5.3 on HP FOCUS hardware. The operating systems were built on top of a common kernel, called **SUNOS** (no relation to Sun Microsystems' SunOS Unix) which provided basic operating primitives like memory, processor and I/O management. This was intended to be invisible to the user; the Unix operating system on top ran as a single process on it.

There were three revision of SUNOS:

SUN I OS:

- Kernel for BASIC language system on Dawn (the 9000/520)
- Single user
- No virtual memory
- Supports only HP "Focus" (*i.e.*, HP's own) memory boards
- Only for HP 9000/520

SUN II OS:

- Supports both HP BASIC and HP-UX (at that time a port of System **III** Unix)
- Multiple users
- Virtual memory

- Supports only HP "Focus" (*i.e.*, HP's own) memory boards
- For HP 9000/520, 530 and 540

SUN III OS:

- Updates for new hardware
- Multiple users
- Virtual memory
- Supports both HP "Focus" (*i.e.*, HP's own) and commercial third-party memory boards
- For HP 9000/520, 530, 540 and 550

HP-UX for the 9000/500 was the first commercial UNIX supporting a multi-processor, multi-user system.

3.28.6 References

Manuals

- HP 9000 Series 500 Computers Models 520, 530, 540, 550 Hardware Technical Data (.pdf) Hewlett Packard (November 1984. Accessed 15 January 2008 at hpmuseum.net)
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Other

- Hewlett-Packard 9000 Series 520 Frank McConnell (1997. Accessed January 2008)
- HP Computer Museum - Technical Desktops - 9000/520 Jon Johnston (n. d.: WordSong Communications P/L. Accessed 15 January 2008 and December 2019)
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3.29 Early PA-RISC Systems

3.29.1 Overview

The first PA-RISC systems were released in the 1980s in the HP 9000/800 Series, which were all server systems, although some had graphics capabilities. Both the technical and marketing landscape was changing in the 1980s, as HP had many other server and microcomputer series that it was selling. RISC and Unix servers were both new and rather a niche.

3.29.2 First PA-RISC server

The first commercial PA-RISC product appeared in 1986 with the **HP 9000/840** "Indigo" computer, based on a six-board TTL implementation of the 32-bit PA-RISC 1.0 architecture, TS-1, running at 8 MHz. The TTL boards measure 8.4×11.3″, SRAMs/PALs and about 150 ICs each. The TS-1 boards implement the processor pipeline, a 4096-entry TLB and 128 KB L1 cache, divided into 64 KB for each data and instruction.[2]

Two main buses are used in the I/O system: Central Bus CTB, also called MidBus, connects the processor to the main memory and the secondary I/O bus. CTB is 32-bit wide and has a clock speed of 8 MHz, with a sustained transfer rate of 20 MB/s. Seven slots for general purpose I/O cards are available. Channel I/O CIO is the central device I/O bus, with up to three CIO channels (CIB) in a single 9000/840 computer. CIO/CIB is 16-bit wide and achieves a transfer rate of 5 MB/s with a clock speed of 4 MHz, with seven shared I/O slots. Supported devices on CIO include HP-IB, the "Hewlett-Packard Interface-Bus", used for instrumentation, measurement and networking adapters.

Up to 112 MB of RAM was supported: 7×16 MB with 2-16 MB memory modules compatible. The optional graphics adapter used one I/O and one memory slot, reducing the maximum RAM to 96 MB. Included by default into the system was a separate Floating Point Coprocessor (FPC) board. The 840 could be upgraded via a CPU board swap to 825, 835 or 845s retaining the case and memory and I/O boards.

The HP 9000/840 achieved about 4.5 MIPS and ran HP-UX version 1.0 (heavily BSD-based) until version 10.01, the pre-Y2k release. Storage and media devices were attached to HP-IB, SCSI was available only later and with newer boot ROMs.

3.29.3 NMOS minicomputers

NS-1 processor

Between 1987 and 1988 first systems with 32-bit PA-RISC 1.0 processors implemented in NMOS-III NS-1 were released:[3] The HP 9000/825S minicomputer, 825SRX "Superworkstation", 835 and 850S "Super-minicomputer".

These systems used three main buses, expanding the original 9000/840 architecture:[4] The 64-bit wide System Main Bus SMB connects the CPU, main memory and I/O over CTBs with a throughput of 100 MB/s. Two CTBs/Midbuses attach via two bus converters to the SMB, while the I/O devices attach via CIO/CIBs to the two CTBs.

The **HP 9000/825 or 825S** "FireFox" were slightly smaller servers or minicomputers, also sold as 825SRX "Superworkstation", based on the 25 MHz NS-1 processor on two boards, with 16 KB cache and 2048-entry TLB. Their central CTB buses run at 8.33 MHz with seven shared I/O CIO and memory

slots. Maximum RAM was 112 MB or 96 MB with graphics adapter, which could be expanded with 16MB arrays. The 825 sold for a price of about US $42,500 in 1987, with a performance of about 9 MIPS. It was also sold with graphics hardware as **825CHX**, which included a 2D adapter and **825SRX** with up to 24-bit 3D graphics.

The **HP 9000/835 or 835S** "TopGun" were slighly bigger servers with the 30 MHz NS-1 processor (maybe also NS-2 processor), with 128 KB cache and >4096-entry TLB. Their central CTB buses run at 10 MHz, their maximum, with seven shared I/O CIO and memory slots. Maximum RAM was 112 MB or 96 MB with graphics adapter, which could be expanded with 16MB arrays. The 835 were slightly more expensive, and sold for about US $45,000 in 1988 for a prformance of about 14 MIPS. Similar to other 800s, the 835 were also sold with graphics hardware as **835CHX** with 2D adapter or **835SRX** with up to 24-bit 3D. Special models were the **9000/834**, a standard 835 with a two-user limit and **9000/835SE**, a high-end version with integrated CIO expander. Server versions without graphics were shortly sold as **9000/635SV**.

A port of early PA-RISC HPBSD ran on 834 and 835, as did an unreleased Mach 3.0 port from the University of Utah The Chorus operating system was ported in 1990-1991 to the 834 with v 3.3 nucleus kernel and v3.2 MiX operating system personality on top.

The **HP 9000/850 or 850S** "Cheetah" were bigger cabinet servers with a 27.5 MHz NS-1 processor with 128 KB cache combined I/D and 4096-entry TLB. Their CTBs run at 9.16 MHz, with CIO I/O buses. The 850 additionally had two Memory Array Buses MAB, capable of linking up eight 16 MB memory modules arrays via a 72-bit data path to the SMB. Maximum RAM was 128 MB with one memory controller and 256 MB with two memory controllers. Sold for a price of about US $200,000 in 1987 with a performance of about 14 MIPS.

NS-2 processor

Later, in 1989, similar computers based on the NS-2, a revamped NS-1, appeared from early 1989 till late 1990. These systems are all based on the same I/O architecture and CIO devices and faciliate the same CPU design — the PA-RISC 1.0 NS-2 processor. These PA-RISC 1.0 and CIO servers include the following:[5]

The **HP 9000/845** "ShoGun" from 1989 had a 27.5 MHz NS-2 processor (not sure, could also be based on a NS-1) with 256 KB cache and a 16384-entry TLB. The CTB main buses run at 9.16 MHz for seven shared I/O CIO and memory slots. Maximum RAM of 112 MB: 7×16 MB, 96 MB: 6×16 MB with graphics adapter Performance was about 22 MIPS. Server versions without graphics were shortly sold as **9000/645SV**.

The **HP 9000/855 or 855S** "Jaguar" were slighly bigger servers with a 27.5 MHz NS-2 processor with 256 KB cache and a 16384-entry TLB. CTBs run at 9.16 MHz, maximum RAM is 128 MB with one and 256 MB with two memory controllers. Performance was about 22 MIPS for a price of roughly US $300,000 (!) in 1990.

The **HP 9000/860 or 860S** "Cougar" servers were also cabinet, mainframe-like systems with a 27.5 MHz NS-2 processor with 1024 KB cache and a 16384-entry TLB. CTBs run at 9.16 MHz, maximum RAM is 128 MB with one and 256 MB with two memory controllers. The 860 could be upgraded with newer CPU boards to a 865 or 870 server.

3.29.4 Low-cost servers

Lower-end and more compact servers were introduced between 1989 and 1990, based on the NS-2 processor and PCX processor using the HP-PB I/O bus.[7]

The **HP 9000/822** "SilverFox Low" was the entry model with a 25 MHz NS-2 processor with 32 KB cache and a 4096-entry TLB. Maximum RAM was 128 MB or 64 MB. Performance was about 10 MIPS for a price of around $20,000 in 1989.

The **HP 9000/832** "SilverFox High" was very similar to the 822 but had slighly higher performance with a faster 30 MHz NS-2 processor with 128 KB cache and a 4096-entry TLB. Maximum RAM was either 128 MB or 64 MB. Performance was 15 MIPS for a price of about US $30,000 in 1989.

The **HP 9000/808 and 815** used the same PCX processor and similar system design, with a performance of 7 MIPS. Maximum RAM for the 808 was 32 MB, for the 815 it was 56 MB. The latter was sold in 1990 for around $14,900.

3.29.5 CMOS servers

The HP 9000/842, 9000/852, 9000/865 and the multi-processor 9000/870 include the first PA-RISC processors implemented in CMOS — the PA-RISC 1.0 PCX. These systems are very similar to the NS-2 based servers, with the 860 being board-upgradeable to a 865 or 870, and feature the same principal system and I/O architecture with a slightly modified CPU/SPU design.[6] These system use the same 16 MB memory arrays as earlier servers but could also use 64 MB boards.

The **HP 9000/842** "SilverBullet Low" used a 32 MHz PCX processor with 1024 KB cache and a 8192-entry TLB. Performance was about 30 MIPS for a price of about $85,000 at time of introduction in 1990. The **HP 9000/852** "SilverBullet High" was almost the same design, but with a faster 50 MHz PCX processor for a performance of about 50 MIPS. It also cost more, around $143,000.

The **HP 9000/865** "Panther" server was again a bigger design with a fast 50 MHz PCX processor with 768 KB cache and a 8192-entry TLB. For I/O the CIO bus was used, maximum RAM was 512 MB. It was sold for about $275,000 first released in 1991.

HP 9000/870 or 870s "Panther" was similarly named and the first SMP multiprocessor PA-RISC system with up to four 50 MHz PCX processors with 1024 KB cache and a 8192-entry TLB each. The 870/100 was uni-, 870/200 dual-, 870/300 triple- and 870/400 quad-CPU. The CIO bus was again used for I/O, and maximum RAM was 1024 MB with two memory controllers in 16 slots. Performance was about 50 MIPS for single-CPU and 90 MIPS for dual-CPU, for a price of about $440,000 for 870/300, $530,000 for 870/400.

3.29.6 Benchmarks

Assorted MIPS performance figures for some systems.

Model	MIPS
840	4.5
825	9
822	10
850	14
835	14
832	15

845	22
855	22
842	30
852	50
870/100single	50
870/200 dual	90

3.29.7 References

Information on these early PA-RISC computers is fragmented and inconsistent. This includes official sales and technical documentation, with sometimes divergent accounts of hardware and architecture, plus divergent information on used PA-RISC processors. Much of the information here was pieced together from old news articles and press releases, plus documentation available at the HP Computer Museum.

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2. Wayne E. Holt (ed.), *Beyond RISC! An Essential Guide to Hewlett-Packard Precision Architecture*, p. 95-102. (January 1988: Software Research Northwest Inc.) and Hardware Design of the First HP Precision Architecture Computers (PDF) David A. Fotland et al (March 1987: Hewlett-Packard Journal)
3. HP 3000 Series 950 and HP 9000 Model 850S Family CE Handbook (PDF) Hewlett-Packard Company (October 1990. Accessed January 2008 at hpmuseum.net) and HP 9000 Series 800 Model 825S Hardware Technical Data (PDF) Hewlett-Packard Company (September 1988. Accessed January 2008 at hpmuseum.net) and HP 3000/925 and HP 9000/825/835 Computer Systems CE Handbook (PDF) Hewlett-Packard Company (May 1988. Accessed January 2008 at hpmuseum.net) and New midrange members of the Hewlett-Packard Precision Architecture Computer Family Thomas O. Meyer et al (June 1989: Hewlett Packard Journal. Accessed January 2008 at findarticles.com)
4. Wayne E. Holt, *Beyond RISC!*
5. Hewlett-Packard Company, *HP 3000 Series 950 and HP 9000 Model 850S Family CE Handbook*
6. Ibid.
7. HP 9000 Series 800 Model 822S/832S Technical Data (PDF) Hewlett-Packard Company (1989. Accessed January 2008 at hpmuseum.net)
8. For HP 9000/840: Interview with David Fotland, September/October 2008

3.30 HP 9000 Series 800 Nova Servers

3.30.1 Overview

The HP 9000 800 Nova servers were second-generation 32-bit HP 9000/800 PA-RISC servers from the early 1990s and based on PA-7000 and PA-7100 processors. They were available in different sizes with different expansion options, CPUs and clock speeds, denoted by the following naming convention:

- The first letter [**F, G, H, I**] indicates external features, like casing and expansion
- The number [**10, 20, âĂę, 70**] indicates internal features, like CPU and chipset

They were suceeded in the HP 9000/800 series by the PA-7100LC E-Class servers with a similar case to the F-Class.

Model numbers.

System	Model number
F10	HP 9000/807
F20, H20	HP 9000/817, HP 9000/827
F30, G30/H30, I30	HP 9000/837, HP 9000/847, HP 9000/857
G40/H40, I40	HP 9000/867, HP 9000/877
G50/H50, I50	HP 9000/887, HP 9000/897
G60/H60, I60	HP 9000/887, HP 9000/897
G70/H70, I70	HP 9000/887, HP 9000/897

3.30.2 System

CPU

- F10: PA-7000 32 MHz with 32/64 KB off-chip I/D L1 cache
- F20, H20: PA-7000 48 MHz with 64/64 KB off-chip I/D L1 cache
- F30, G30, H30, I30: PA-7000 48 MHz with 256/256 KB off-chip I/D L1 cache
- G40, H40, I40: PA-7000 64 MHz with 256/256 KB off-chip I/D L1 cache
- G50, H50, I50: PA-7100 96 MHz with 256/256 KB off-chip I/D L1 cache
- G60, H60, I60: PA-7100 96 MHz with 1024/1024 KB off-chip I/D L1 cache
- G70, H70, I70: 1-2 PA-7100 96 MHz with 2048/2048 KB off-chip I/D L1 cache each

Optional FPU in systems with PA-7000 processors the FPU.

Chipset

The chipset a variant of the ASP, with at least the Viper memory controller interfacing the processor to memory and the HP-PB I/O bus. The rest of the system I/O is implemented on so-called HP-PB Personality Boards.

Buses

- PBus processor/memory bus
- VSC main system bus
- HP-PB bus for the general I/O
- SCSI-2 Narrow single-ended bus for main storage I/O

Memory

- HP proprietary modules like on 720, 730 and 750, and 735/755
- F10: 16 MB minimum, 128 MB (8×16 MB) maximum
- F20 and F30: 16 MB minimum, 192 MB (12×16 MB) maximum
- H20, H30, G30, I30, x40: 16 MB minimum, 384 MB (12×32 MB) maximum
- x50, x60, x70: 16 MB minimum, 768 MB (12×64 MB) maximum

Expansion

- Fx0: two HP-PB single-height/one double-height slots
- Gx0: six HP-PB single-height/three double-height slots
- Hx0: six HP-PB single-height/three double-height slots
- Ix0: twelve HP-PB single-height/six double-height slots

Drives

- Many

3.30.3 External

- SCSI-2 50-pin single-ended
- High-pin-count MUX connector
- Parallel DB25
- Rest depends on installed HP-PB cards

3.30.4 Operating systems

The only operating system for these servers was HP-UX, with all of them supported in HP-UX 10.20 for 800s servers and 11.00. First supported release was HP-UX 8.02, official support was dropped in 11.11 (11i v1).

It is unlikely there will ever be a port of an open source operating system, as not much documentation exist on the I/O and system details.

3.30.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	MIPS
F10	22.0	36.6	35
x20	33.6	56.1	53
x30	37.8	62.4	53
x40	65.2	91.3	70
x50	100.0	158.5	115
x60	108.8	195.3	115
x70	108.8	195.3	115

3.30.6 References

Manuals

- Owner's Guide to the HP 9000 8x7S Family (.pdf) Hewlett-Packard Company (1991. Accessed January 2009 at hpmuseum.net)
- CE Handbook Series 9x7 and Model 8x7S Family (.pdf) Hewlett-Packard Company (February 1992, edition E0292, part number A1707-90016. Accessed January 2009 at hpmuseum.net)

Other

- Pinout for the mini-DIN console connector at the back

3.31 HP i2000

3.31.1 Overview

The HP i2000 was HP's first Itanium workstation with a first generation *Merced* Itanium processor as a proof-of-concept to deliver first Itanium hardware, based on an early Intel 82460GX reference design (also rebranded and sold by other vendors). It had certain limitations due to chipset and/or operating system bugs, supported only first generation Itanium CPUs and was rather slow.

3.31.2 System

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1	Itanium 1 *Merced*	733 MHz	16/16 KB	96 KB	2.0 MB or4.0 MB
1-2	Itanium 1 *Merced*	800 MHz	16/16 KB	96 KB	2.0 MB or4.0 MB

L1 and L2 caches are on-die, L3 is off-chip.

Chipset

- Intel 82460GX chipset
- Two WXBs (Wide eXpansion Bridges) for each one PCI 64/66 bus
- PXB (PCI eXpansion Bridge) for one PCI 64/33 bus
- I/O and Firmware Bridge (IFB) communicates to IDE, USB and Super I/O
- Qlogic 12160 dual-channel Ultra3 SCSI controller (separate PCI card, standard configuration)
- Intel 82559 Fast Ethernet controller
- nVIDIA Quadro2 Pro video card (separate AGP card, standard configuration)
- ATA-33 IDE controller (on IFB)
- USB controller (on IFB)
- LPC47B27 Super I/O (serial and PS/2 ports controller)

Buses

- Memory bus, 266 MHz, 4.2 GB/s peak
- Two PCI 64/66 I/O buses (for expansion slots)
- PCI 64/33 I/O bus (for expansion slots)
- PCI 32/33 I/O bus (for onboard devices)

Memory

- PC100 registered SDRAM DIMMs
- Up to two memory expansion cards (MECs)
- Eight slots on each MEC
- Up to 1 GB modules
- 16 GB maximum (16×1 GB — 8 GB on each MEC)

Expansion

- Five PCI 64-bit/66 MHz slots, 3.3 V
- Two PCI 64-bit/33 MHz slots, 5 V
- One AGP Pro 110 slot (supports AGP-1x, 3x, 4x, or AGPpro-110)

Drives

- Three (1.6âĂș) or five (1âĂș) internal 3.5âĂș bays for hard drives
- Three half-heigth 5.25âĂș bays for externally accessible drives
- One 3.5âĂș bay for externally accessible drive (standard shipped with a LS-120 drive)

3.31.3 External

- 10/100 Ethernet TP/RJ45
- Four USB ports (two on front, two on rear)
- Serial RS232C DB9
- Two PS/2 for keyboard and mouse
- Three phone jacks (microphone, line-in and line-out)

3.31.4 Operating systems

- HP-UX 11i v1.5 and v1.6
- Linux for Itanium
- FreeBSD/ia64
- Windows XP 64-Bit Edition Version 2003
- Windows XP Professional 64-bit Edition
- Windows 2000 Server IA64 Edition (Beta Release)
- Windows Server 2003 Itanium-based Editions

3.31.5 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000*rate*, int	SPEC2000*rate*, fp
i2000733 MHz 2 MB		623		7.2
i2000733 MHz 4 MB		577		
i2000800 MHz 2 MB		6552-CPU: 658		7.6 2-CPU: 13.2
i2000800 MHz 4 MB	365	610		

3.31.6 Dimensions

Height	Width	Depth	Weight
457mm	254mm	645mm	38kg

3.31.7 References

Manuals

- HP Workstation i2000 Owner's Guide (URL gone)

3.32 HP Visualize J200, J210, J280, J2240

3.32.1 Overview

The HP Visualize J-Class were multi processor-capable large PA-RISC workstations from the mid-1990s in deskside chassis with interlocked modules. A variety of 32- and 64-bit processors were available in the different machines – the J200 and J210 were 32-bit, the J280, J282 and J2240 were 64-bit. The J280 is only a single-processor machine, which can be upgraded to a dual-capable J282.

Model numbers:

- J200, J210, J210XC: HP 9000/770
- J280, J282: HP 9000/780
- J2240: HP 9000/782

3.32.2 System

CPU

- J200: 1-2 PA-7200 100 MHz with 256/256 KB off-chip I/D L1 and 2 KB on-chip "assist" L1 cache
- J210: 1-2 PA-7200 120 MHz with 256/256 KB off-chip I/D L1 and 2 KB on-chip "assist" L1 cache
- J210XC: 1-2 PA-7200 120 MHz with 1/1 MB off-chip I/D L1 and 2 KB on-chip "assist" L1 cache
- J280: 1 PA-8000 180 MHz with 1/1 MB off-chip I/D L1 cache
- J282: 1-2 PA-8000 180 MHz with 1/1 MB off-chip I/D L1 cache
- J2240: 1-2 PA-8200 236 MHz with 2/2 MB external I/D L1 cache

Chipset

- PA-7200-models: U2 I/O adapter Runway to GSC bridge
- PA-8000/PA-8200-models: UTurn I/O adapter Runway to GSC bridge
- MMC/SMC memory controllers
- LASI I/O chipset
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Wax EISA bridge
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- Other I/O (serial, parallel, Floppy, HP-HIL)
- J2240: Dino GSC-to-PCI bridge

- J2240: Cujo GSC-to-PCI bridge, 64-bit
- J2240: Symbios Logic 53C895 16-bit Ultra-Wide SCSI-2 controller
- J2240: DEC 21142/43 (*Tulip*) Fast-Ethernet controller

Buses

- Runway CPU/memory bus (100 MHz with 800 MB/s peak data rate on J200, 120 MHz 960 MB/s on all others)
- Cache:
  - J200: 64-bit wide, 800 MB/s I-fetch (8-Byte), 800 MB/s D-load (16-Byte), 800 MB/s single D-store (8-Byte)
  - J210/J210XC: 64-bit wide, 960 MB/s I-fetch (8-Byte), 960 MB/s D-load (16-Byte), 960 MB/s single D-store (8-Byte)
  - J280/J282: 128-bit wide, 2.88 GB/s I-fetch, 2.88 GB/s D-load (16-Byte), 1.44 GB/s D-store (8-Byte)
- GSC system level I/O bus
- EISA additional expansion I/O bus
- SCSI-2 Fast-Wide *high-voltage differential* bus; main storage I/O
- SCSI-2 Fast-Narrow single-ended bus
- J2240: SCSI-3 Ultra-Wide single-ended bus; main storage I/O
- J2240: PCI bus;

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- J200: 800 MB/s peak bandwidth
- J210: 960 MB/s peak bandwidth
- 16 slots for 16-128 MB modules
- 32 MB to 2 GB supported
- J2240: 4 GB maximum (with 256 MB modules)

Expansion

- One slot for a GSC (EISA formfactor) card
- Two slots for EISA cards

- Two slots for GSC (EISA formfactor) or EISA cards
- Slot layout, from bottom to top:
  1. GSC (for primary graphics)
  2. EISA or GSC
  3. EISA or GSC
  4. EISA
  5. EISA

J2240:

- One slot for a PCI 32-bit/33 MHz, 5 V card
- One slot for a PCI 32-bit/33 MHz, 5 V or EISA card
- One slot for a GSC or PCI 32-bit 32-bit/33 MHz, 5 V card
- Two slots for GSC or PCI 64-bit/66 MHz, 3.3 V cards
- Slot layout, from bottom to top:
  1. PCI-64/66, 3.3 V or GSC (for primary graphics)
  2. PCI-32/33, 5 V or GSC
  3. PCI-64/66, 3.3 V or GSC
  4. PCI-32/33, 5 V
  5. PCI-32/33, 5 V or EISA

Drives

- One tray for two 3.5âĂş Fast-Wide HVD 68-pin SCSI hard drives
- One tray for two half-heigth 5.25âĂş Fast-Narrow SE 50-pin SCSI drives, external accessible

3.32.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- SCSI-3 68-pin Fast-Wide *high-voltage differential* (HVD)
- J2240: SCSI-3 68-pin Ultra-Wide single-ended
- Two Serial RS232C DB9 (up to 460.8Kb/s)
- Parallel DB25
- Ethernet RJ45 /
- J2240: Fast Ethernet RJ45
- Ethernet AUI 15-pin
- Graphics port depends on installed framebuffer

- Two PS/2 connectors for keyboard & mouse
- HP-HIL for input device loop
- Four phone jacks (microphone, headphones, line-in and ?)

3.32.4 Operating systems

- HP-UX: 10.20, 11.00 and 11i v1
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.32.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
J200	4.98	4.50	44.8	61.3
J200 2-CPU			64.5	105
J210	6.00	5.40	54.0	73.4
J210 2-CPU			77.5	126
J210XC	6.40	5.70	57.6	81.5
J210XC2-CPU			82.8	142
J280	11.80	19.30		
J282	?	?		
J2240	17.40	26.30	157	237
J2240 2-CPU			307	349

3.32.6 Dimensions

Height	Width	Depth	Weight
470mm	330mm	541mm	50kg

3.32.7 References

Manuals

- Visualize J200, J210 technical reference manual (URL gone)
- Visualize J280 Owner's Guide (URL gone)
- Visualize J280 workstation upgrade instructions (URL gone)
- Visualize J280, J282, J2240 Service Handbook (URL gone)
- Visualize J282, J2240 Owner's Guide (URL gone)
- Visualize J282 workstation upgrade instructions (URL gone)
- Visualize J2240 workstation upgrade instructions (URL gone)

Articles

- Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost (.pdf) William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996: Hewlett-Packard Journal)
- A New Memory System Design for Commercial and Technical Computing Products (.pdf) Thomas R. Hotchkiss, Norman D. Marschke, and Richard M. McClosky (Februar 1996: Hewlett-Packard Journal)

Other

- Replacing the EEPROM on an HP Visualize J282 (URL gone)

3.33 HP Visualize J5000, J5600, J7000, J7600

3.33.1 Overview

These HP Visualize J-Class workstations were aimed at the graphics workstations market, equipped with up to two 64-bit PA-8500 processors with large on-chip L1 caches. They are basically the bigger brothers of the C3000/C3600 et al, featuring better expandability. The architecture was a major change from its predecessors with new I/O devices and no LASI I/O chip or GSC bus anymore. All device I/O now attach to PCI buses, external I/O devices are connected to USB ports.

Model numbers: all have the HP 9000/785 model number.

3.33.2 System

CPU

- J5000: 1-2 PA-8500 440 MHz with 512/1024 KB on-chip I/D L1 cache each
- J5600: 1-2 PA-8600 552 MHz with 512/1024 KB on-chip I/D L1 cache each
- J7000: 1-4 PA-8500 440 MHz with 512/1024 KB on-chip I/D L1 cache each
- J7600: 1-4 PA-8600 552 MHz with 512/1024 KB on-chip I/D L1 cache each

Chipset

- Astro memory/Runway controller
- Four Elroy PCI bridges
- National 87560 *(SuperI/O)*, handling USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Runway CPU/memory bus
- PCI-64/33 high-performance device I/O bus
- PCI-64/66 high-performance graphics I/O bus
- SCSI-2 Ultra-Narrow single-ended bus
- SCSI-3 Ultra2-Wide LVD bus main storage I/O
- IDE bus; CD/floppy I/O

Memory

- 278-pin 120 MHz ECC SDRAM DIMMs
- Takes 256/512/1024 MB modules
- J5000: 8 slots
- J7000: 16 slots
- 256 MB (1×256) minimum, J5000: 8 GB (8×1024) maximum; J7000: 16 GB (16×1024) maximum.

Expansion

- Five PCI 64-bit/33 MHz, 5 V slots
- Two PCI 64-bit/66 MHz, 3.3 V slots
- I/O slots layout (from top to bottom):
  1. EMPTY
  2. PCI-64/33, 5 V
  3. PCI-64/33, 5 V
  4. PCI-64/66, 3.3 V
  5. PCI-64/33, 5 V
  6. PCI-64/33, 5 V
  7. PCI-64/66, 3.3 V
  8. PCI-64/33, 5 V

Drives

- Four SCSI 3.5âĂş Ultra2-Wide LVD hard drives with 80-pin SCA connector
- 3.5âĂş Floppy drive
- SCSI half-heigth 5.25âĂş drive, external accessible

3.33.3 External

- SCSI-2 50-pin Ultra-Narrow single-ended
- SCSI-3 68-pin Ultra2-Wide LVD
- Two Serial RS232C DB9
- Parallel DB25
- Fast Ethernet RJ45
- Two USB ports for keyboard & mouse

- Four phone jacks (microphone, headphones, line-in and line-out)

3.33.4 Operating systems

- HP-UX: 10.20 , 11.0011i v1 (both only 64-bit releases)
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.33.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95 *rate*, int	SPEC95 *rate*, fp	SPEC2000, int	SPEC2000, fp
J5000	32.50	54.00	302	486		
J5000 2-CPU			579	744		
J5600	42.60	62.70	384	564	408	392
J5600 2-CPU			758	847		
J7000	32.50	54.00	302	486		
J7000 2-CPU			579	744		

3.33.6 References

Manuals

- J5x00/J7x00 Owner's Guide (PDF, 4.5 MB)
- J5x00/J7x00 Service Handbook (PDF, 4.4 MB)
- VISUALIZE Workstation Memory Subsystem (PDF, 120 KB)

3.34 HP Visualize J6000, J6700

3.34.1 Overview

These HP Visualize J-Class computers were small RISC workstations were aimed at the Unix graphics market, equipped with the new 64-bit PA-8600 and PA-8700, both featuring large on-chip L1 caches. The architecture was a major change from those of its predecessors. New I/O devices were integrated, the LASI I/O chip was removed together with the old GSC bus. All devices now attach to PCI buses, I/O devices are connected to USB ports. The case can be used on the desktop or fitted in a 19âĂş rack with 2U space.

Model numbers: all have the HP 9000/785 model number.

3.34.2 System

CPU

- J6000: 1-2 PA-8600 552 MHz with 512/1024 KB on-chip I/D L1 cache
- J6700: 1-2 PA-8700 750 MHz with 768/1536 KB on-chip I/D L1 cache
- J6750: 1-2 PA-8700+ 875 MHz with 768/1536 KB on-chip I/D L1 cache

Chipset

The system is built around the HP Astro chipset:

- HP **Astro** chipset
  - **Astro memory and I/O controller** connects to the two processors via the Runway processor bus (2.0 GB/s), the memory bus (2.0 GB/s) and eight I/O channels ("ropes" — aggregate 2.0 GB/s) and contains both memory, I/O and cache controllers
  - Four **Elroy PCI bridges** connect the PCI slots and I/O devices on the onboard PCI bus to the Astro with an aggregate bandwidth of 2.0 GB/s on seven I/O channels (one of the eight channels of the Astro controller is unused)
    1. PCI 64/66 I/O slot on two channels — 0.5 GB/s
    2. PCI 64/66 I/O slot on two channels — 0.5 GB/s
    3. PCI 64/66 I/O slot on two channels — 0.5 GB/s
    4. Onboard I/O devices (Fast Ethernet, SCSI, audio, IDE/USB etc.) on one channel — 250 MB/s
- National 87560 ("Super I/O"), integrates USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip
- DEC 21142/43 Fast Ethernet controller *(Tulip)*

- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Runway CPU bus with 2.0 GB/s
- Memory bus, about 2.0 GB/s
- I/O bandwidth of around 1.75 GB/s
- Three PCI-64/66 buses for expansion slots
- PCI-64/33 bus for onboard I/O devices
- SCSI-3 Ultra2-Wide LVD buses main storage I/O
- IDE bus for CD/DVD removable media

Memory

- 278-pin 120 MHz ECC SDRAM DIMMs
- 16 slots for 512 MB/1 GB DIMMs
- 1 GB to 16 GB supported

Expansion

- Three PCI 64-bit/66 MHz, 3.3 V slots

Drives

- Two SCSI 3.5âĂș Ultra2-Wide LVD hard drives with 80-pin SCA connector
- Slim-line ATAPI CD-ROM

3.34.3 External

- SCSI-3 68-pin Ultra2-Wide LVD connector (SE)
- Two Serial RS232C DB9
- Parallel DB25
- Fast Ethernet RJ45
- Two USB ports for keyboard & mouse
- Four phone jacks (microphone, headphones, line-in and line-out)

3.34.4 Operating systems

- HP-UX: 10.20 (J6000), 11.00, and 11i v1 (both only 64-bit releases)
- Linux
- OpenBSD (32-bit)
- NetBSD (32-bit)

3.34.5 Benchmarks

Model	**SPEC95, int**	**SPEC95, fp**	**SPEC95 *rate*, int**	**SPEC95 *rate*, fp**	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
J6000	42.60	62.70	384 2-CPU: 758	564 2-CPU: 847	441	433	2-CPU: 9.7	2-CPU: 8.0
J6700	57.60	85.90			603	581	2-CPU: 13.4	2-CPU: 10.5
J6750					676	651	2-CPU: 14.9	2-CPU: 11.5

3.34.6 References

Manuals

- J6000 Service Handbook (PDF, 4.5 MB)
- J6000 Technical Reference (URL gone)
- J6700 Service Handbook (URL gone)
- J6700 Technical Reference (URL gone)

3.35 HP 9000/K-Class

3.35.1 Overview

The HP 9000 K-Class are multiprocessor PA-RISC servers from the mid- to late-1990s, part of the HP 9000 800 series of servers. They based on the U2/UTurn chipset architecture and Runway-based PA-7200 and PA-8000 processors. The K200s and K400s were up to four-way, the K370/K380 and K570/K580 up to six-way SMP. A typical K-Class server consists of a System Processing Unit (SPU), seperate system console and an optional UPS, bundled into a single 19âĂş rack.

In the 1990s, D-Class servers were part of the US Navy TAC-4 program, in which HP was a vendor supplying RISC Unix computers for uses throughout the Navy. The D-Class were part of a technology refreshment of TAC-4 in 1996.

The K-Class naming convention for server types is as follows.

- The first digit after "K" , **1-5**, indicates the server type:
  - K100: single-CPU with limited expandability
  - K2x0: up to four CPUs, better expandability and memory
  - K3x0: up to six CPUs and more I/O slots
  - K4x0: up to four CPUs, more I/O slots and more memory
  - K5x0: up to six CPUs and a different I/O configuration
- The number after that, **00, 10, âĂę 80** indicates the system design with CPUs and chipset.
  - 00/10/20: PA-7200 processor and UTurn architecture
  - 50/60: PA-8000 processor and U2 architecture
  - 70/80: PA-8200 processor and U2 architecture

System	Model number	Introduced
K100, K200, K400	HP 9000/809, HP 9000/819, HP 9000/829	March 1995
K210, K410	HP 9000/839, HP 9000/849	September 1995
K220, K420	HP 9000/859, HP 9000/869	March 1996
K250, K450	HP 9000/802, HP 9000/804	August 1996
K260, K460	HP 9000/879, HP 9000/889	August 1996
K370, K570	HP 9000/898, HP 9000/899	May 1997
K380, K580	HP 9000/800	February 1998

3.35.2 System

CPU

- K100: PA-7200 100 MHz with 512 KB off-chip L1 and 2 KB on-chip L1 cache
- K200/K400: 1-4 PA-7200 100 MHz with 512 KB off-chip L1 and 2 KB on-chip L1 cache each
- K210/K410: 1-4 PA-7200 120 MHz with 512 KB off-chip L1 and 2 KB on-chip L1 cache each
- K220/K420: 1-4 PA-7200 120 MHz with 2 MB off-chip L1 and 2 KB on-chip L1 cache each

- K250/K450: 1-4 PA-8000 160 MHz with 2 MB off-chip L1 cache each
- K260/K460: 1-4 PA-8000 180 MHz with 2 MB off-chip L1 cache each
- K370/L570: 1-6 PA-8200 200 MHz with 4 MB off-chip L1 cache each
- K380/K580: 1-6 PA-8200 240 MHz with 4 MB off-chip L1 cache each

Chipset

- *PA-7200*U2 I/O adapter Runway to GSC bridge
- *PA-8000/8200*UTurn I/O adapter Runway to GSC bridge
- MMC/SMC memory controllers
- Gecko BOA BC GSC+ Port
- LASI I/O chipset
- NCR 53C710 8-bit single-ended SCSI-2
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Eole CAP/MUX
- Other I/O (serial, parallel)

Buses

- Runway CPU/memory bus, 100 MHz with 800 MB peak on Kx00, 120 MHz 960 MB/s on all others
- GSC+ bus for general system level I/O
- HSC bus for expansion I/O
- HP-PB bus for expansion I/O
- SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage I/O
- SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Memory

- *K100* 512 MB maximum RAM
- *K200, K210, K220* 2 GB maximum RAM
- *K250, K260, K370, K380, K400, K410, K420* 4 GB maximum RAM
- *K450, K460, K570, K580* 8 GB maximum RAM
- 72-pin ECC SIMMs on special RAM boards

- Systems with a PA-8x00 need 50ns access time modules, PA-7200 models can take up to 60ns. Slower modules could work.

Expansion

- One slot for a GSC/HSC card on the core I/O board
- Four slots for HP-PB cards
- *K3x0* With a 2-slot HSC I/O expansion module two more GSC/HSC cards could be used
- *K4x0 and K4x0* With a 2- or 4-slot HSC I/O expansion module two or four more GSC/HSC cards could be used
- *K4x0* Four more HP-PB slots (eight in all)

Drives

- One tray for four Fast-Wide 68-pin SCSI-2 high-voltage differential hard drives
- One vertical tray for two 5.25âĂş half-height drives, external accessible

3.35.3 External

- 68-pin HD SCSI-2 Fast-Wide high-voltage differential
- TP/RJ45 10BaseT 10 Mbit Ethernet
- Ethernet AUI 15-pin
- Two Serial RS232C DB9, one for console, one for UPS
- DB25 male RS232C serial, for remote console via modem
- Parallel DB25
- Two PS/2 connectors for keyboard und mouse
- MDP-connector for a serial MUX
- *Kx50/Kx60/Kx70/Kx80* Four audio jacks

3.35.4 Operating systems

- HP-UX 10.20 for 800s servers, HP-UX 11.00 and 11i v1
- Linux: most models
- OpenBSD: K100, K200, K210, K220, K400, K410, K420
- NetBSD: K100, K200, K210, K220, K400, K410, K420

3.35.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
Kx00	4.92	6.80	44.3	61.2
Kx002-CPU			87.9	117
Kx004-CPU			174	198
Kx10	5.92	8.15	53.3	73.4
Kx102-CPU			106	140
Kx104-CPU			210	238
Kx20	6.41	9.11	57.7	82.0
Kx202-CPU			114	157
Kx204-CPU			228	275
Kx50	10.7	18.8	96.	169
Kx502-CPU			189	279
Kx504-CPU			375	383
Kx60	11.8	20.2	107	182
Kx602-CPU			212	297
Kx604-CPU			418	398
Kx70	14.6	23.0	132	207
Kx702-CPU			261	322
Kx704-CPU			519	434
Kx706-CPU			767	489
Kx80	17.4	28.5	157	257
Kx802-CPU			312	398
Kx804-CPU			610	532
Kx806-CPU			902	604

3.35.6 Dimensions

Model	Height	Width	Depth	Weight
Stand-alone	635mm	432mm	698mm	59kg
Packaged	870mm	889mm	775mm	77kg

3.35.7 References

Manuals

- Service Manual HP 9000 K-Class Enterprise Servers and HP 3000 Model 9x9KS (PDF, 2.1 MB)
- K-Class Installation Guide (HP 9000/Kxx0) (PDF)
- K-Class Installation Guide (HP 3000/9x9KS) (PDF)
- K-Class Owner's Guide (PDF)

Articles

- Symmetric Multiprocessing Workstations and Servers System-Designed for High Performance and Low Cost (.pdf) William R. Bryg, Kenneth K. Chan, and Nicholas S. Fiduccia (February 1996:

Hewlett-Packard Journal)

◇ J/K-Class Memory System description (PDF, HP Journal 2/96)

3.36 HP L1000 and L2000 (rp5400/rp5450)

3.36.1 Overview

The HP 9000 L-Class L1000 and L2000 are two or four-way multi-processor PA-RISC servers for rack-mounting, 7U in height. They are based on 64-bit processors, and a rather conservative system architecture with an Astro/Elroy system design used in many HP Visualize workstations, such as B2000, C3000 and C3600. As with other HP 9000 servers of the late-1990s, the L-Class were renamed under the **rp** server moniker, but still part of the HP 9000 series. Their L1500 and L3000 sucessors used a completely different system architecture.

The L1000 and L2000 could be upgraded with a board-swap (mainboard, processors, etc.) to the Itanium 2-based rx5670 servers.

Model	rp	Introduced	Price
L1000	rp5400	1999	$16,000
L2000	rp5450	1999	$21,000

3.36.2 System

CPU

The L1000/rp5400 systems support up to 2-way and the L2000/rp5450 up to 4-way SMP. The following table lists the various suffixes denoting the different theoretically possible CPU-configurations. Upgrading from one configuration to another could require the replacement of other parts besides the processor, *e.g.*, the mainboard or power supply.

- -36: PA-8500 360 MHz with 512/1024 KB on-chip I/D L1 cache each
- -44: PA-8500 440 MHz with 512/1024 KB on-chip I/D L1 cache each
- -5X: PA-8600 550 MHz with 512/1024 KB on-chip I/D L1 cache each

Both the L1000 and L2000 came with two different system boards (A and B), which supported different types of processors.

- L1000 (rp5400): up to two CPUs, with the processor type depending on the exact model number:
  - A5576**A:** 360 MHz and 440 MHz processors
  - A5576**B:** 360 MHz, 440 MHz and 550 MHz processors
- L2000 (rp5450): up to four CPUs, with the processor type depending on the exact model number:
  - A5191**A:** 360 MHz and 440 MHz processors
  - A5191**B**: 360 MHz, 440 MHz and 550 MHz processors

Chipset

- Astro memory/Runway controller, connects the memory, CPU bus and I/O
- Eight Elroy PCI bridges
- Two HP Diva Serial [GSP] Multiport UARTs

- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Two Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Runway CPU bus, 82.5 MHz with 1.36 GB/s bandwidth for up to four CPUs
- Memory bus, 1.36 GB/s
- Eight I/O data channels, each 133 MHz 256 MB/s — 2.1 GB/s aggregate
- Two PCI-64/33 I/O buses
- Six PCI-64/66 I/O buses
- SCSI-2 Ultra-Narrow single-ended bus
- Two SCSI-3 Ultra2-Wide LVD main storage I/O buses

Memory

- ECC SDRAM DIMMs
- Take 256 MB/512 MB modules
- 16 slots *(8 of these slots are disabled on L1000s, namely slots 4a/b, 5a/b, 6a/b and 7a/b)*
- 256 MB (1×256) minimum, L1000: 8 GB (8×1 GB) maximum; L2000: 16 GB (16×1 GB) maximum.

Expansion

- Six PCI 64-bit/33 MHz slots on two independent buses:
  - pci0: Slots 1 and 2 are reserved for the Core I/O cards
  - pci1: Slots 3, 4, 5 and 6
  - All of the above slots are not hot-plug capable
- Six PCI 64-bit/66 MHz slots, each on an independent bus. These are hot-plug capable.
- *On L1000s only the slots 1, 2, 3, 8, 9, 10, 11 and 12 are usable!*
- Slot layout (from bottom to top):
  1. PCI-64/33, pci0, reserved for core I/O
  2. PCI-64/33, pci0, reserved for core I/O
  3. PCI-64/33, pci1
  4. PCI-64/33, pci1
  5. PCI-64/33, pci1

6. PCI-64/33, pci1
7. PCI-64/66, pci2, hot-pluggable
8. PCI-64/66, pci3, hot-pluggable
9. PCI-64/66, pci4, hot-pluggable
10. PCI-64/66, pci5, hot-pluggable
11. PCI-64/66, pci6, hot-pluggable
12. PCI-64/66, pci7, hot-pluggable

Drives

- Four trays for each one 3.5âĂş Ultra2-Wide LVD SCSI hard drive with 80-pin SCA connector
- One tray for a half-heigth 5.25âĂş 50-pin Ultra-Narrow SE SCSI drive, external accessible

3.36.3 External

- SCSI-2 50-pin Ultra-Narrow single-ended
- 68-pin VHDI SCSI-3 Ultra2-Wide LVD
- Serial RS232C DB9
- Fast Ethernet RJ45
- Ethernet RJ45 *Web Console*

3.36.4 Operating systems

- HP-UX: 64-bit 11.00, 11i v1 and 11i v2
- Linux: works.

3.36.5 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC2000, int	SPEC2000, fp
L2000-44	33.70	47.20	?	?

3.36.6 Dimensions

Model	Height	Width	Depth	Weight
	368mm	482mm	774mm	68kg
Rack-mounted	7U	482mm	774mm	68kg

3.36.7 References

Manuals

- rp5400 User Guide (URL gone)

3.37 HP L1500 and L3000 (rp5430/rp5470)

3.37.1 Overview

The second version of the HP 9000 L-Class Unix servers are multi-processor servers based on the Stretch chipset, also used in the rp7400 N4000 servers. They are similar to tge L1000 and L2000, 7U rack-mountable with up to two or four processors, 8 GB or 16 GB RAM and a large set of I/O options and expandability.

The L1500 has the same chassis and mainboards as the L3000, but with some of I/O, memory and processors sockets deactivated in hardware, limiting the L1500 to about half of the L3000's capacity. Both could be upgraded with to Itanium 2-based rx5670 servers.

These systems only run 64-bit versions of HP-UX: 11.00 and 11i v1 and v2.

Model	rp	Introduced	Price
L1500	rp5430	2000	
L3000	rp5470	2000	$39,000

3.37.2 System

CPU

The rp5430 (L1500) support up to 2-way and the rp5470 (L3000) up to 4-way multi-processing (SMP). There are several classes of possible processors, both shipped with the systems or later upgraded.

Processor types are indicated with the following suffixes:

- -5X: PA-8600 550 MHz with 512/1024 KB on-chip I/D L1 cache each
- -6X: PA-8700 650 MHz with 768/1536 KB on-chip I/D L1 cache each
- -7X: PA-8700 750 MHz with 768/1536 KB on-chip I/D L1 cache each
- -8X: PA-8700+ 875 MHz with 768/1536 KB on-chip I/D L1 cache each

Both the L1500 and L3000 came with different system boards supporting different processors:

- L1500 (rp5430): up to two CPUs, system boards support all processors from 550 MHz to 750 MHz
- L3000 (rp5470): up to four CPUs, with the processor type depending on the exact model number [unsure which models support the 875 MHz PA-8700+]:
  - A6144A: 550 MHz processors
  - A6144B: 550 MHz, 650 MHz and 750 MHz processors
  - A6840A: 550 MHz, 650 MHz and 750 MHz processors
  - A8328A: 550 MHz, 650 MHz and 750 MHz processors

Chipset

The chipset is based around the Stretch chipset:

- Prelude memory controller, the main crossbar of the system
- DEW Runway converters, attach the CPUs to the system bus
- IKE I/O controller connects the PCI bridges to the system main bus
- *rp5430* Seven Elroy PCI bridges, attach PCI buses to the IKE I/O controller
- *rp5470* Ten Elroy PCI bridges, attach PCI buses to the IKE I/O controller
- DEC 21142/43 Fast Ethernet controller (Tulip)
- Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Two Itanium system buses, 133 MHz DDR, each 2.1 GB/s peak, combined 4.3 GB/s aggregate. Both system buses connect to the central Prelude memory controller.
  1. system bus connects I/O and two CPUs
  2. system bus connects two CPUs.
- Runway+/Runway DDR CPU buses, each 2.1 GB/s peak. Either two or four buses depending on the number of CPUs, with a combined aggregate 4.3 or 8.6 GB/s
- Two memory bused with combined 4.3 GB/s peak. 133 MHz DDR at 64-bit with ECC
- *rp5430*
  - Eight I/O channels, each 133 MHz 256 MB/s — 2.1 GB/s aggregate
  - Five PCI-64/66 I/O buses for expansion slots
  - One PCI-64/33 I/O bus for core I/O
- *rp5470*
  - Twelve I/O channels, each 133 MHz 256 MB/s — 3.2 GB/s aggregate
  - Eight PCI-64/66 I/O buses for expansion slots
  - Two PCI-64/33 I/O buses for expansions slots and core I/O
- SCSI-2 Ultra-Narrow single-ended bus
- Two SCSI-3 Ultra2-Wide LVD main storage I/O buses

Memory

- ECC SDRAM DIMMs
- 256 MB, 512 MB and 1 GB modules supported
- 16 slots
- *rp5430* 8.0 GB maximum (the system will not boot if more than 8.0 GB of memory is installed)
- *rp5470* 16.0 GB maximum

Expansion

- Two "Twin-Turbo" PCI 64-bit/66 MHz slots, each on an independent PCI bus, each connected via two I/O channels (aggregate 512 MB/s), hot-plug capable
- *rp5430*
  - Four "Turbo" PCI 64-bit/66 MHz slots on three PCI buses, each connected via one I/O channel (256 MB/s), three of four slots are hot-plug capable
- *rp5470*
  - Six "Turbo" PCI 64-bit/66 MHz slots, each on an independent PCI bus, each connected via one I/O channel (256 MB/s), hot-plug capable [two of these slots are not active on the rp5430]
  - Two PCI 64-bit/33 MHz slots on a shared bus, on one I/O channel (256 MB/s) [these slots are not active on the rp5430]
- Two PCI 64-bit/33 MHz slots, reserved for LAN/SCSI and GSP (management) cards, on a shared bus, on one I/O channel (256 MB/s)
- All PCI slots are 5 V keyed
- Slot layout (counted from bottom up):
  1. PCI-64/33, pci0, reserved (LAN/SCSI)
  2. PCI-64/33, pci0, reserved (GSP)
  3. PCI-64/33, pci1, shared [not available on rp5430]
  4. PCI-64/33, pci1, shared [not available on rp5430]
  5. PCI-64/66, pci2, Turbo, hot-pluggable [not available on rp5430]
  6. PCI-64/66, pci3, Turbo, hot-pluggable [not available on rp5430]
  7. PCI-64/66, pci4, Turbo, hot-pluggable
  8. PCI-64/66, pci5, Turbo, hot-pluggable
  9. PCI-64/66, pci6, Turbo, hot-pluggable
  10. PCI-64/66, pci7, Turbo, hot-pluggable
  11. PCI-64/66, pci8, Twin-Turbo, hot-pluggable
  12. PCI-64/66, pci9, Twin-Turbo, hot-pluggable

Drives

- Four trays for 3.5âĂş Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector, hot-plug
- One tray for a half-heigth 5.25âĂş 50-pin Ultra-Narrow SE SCSI drive, external accessible

3.37.3 External

- SCSI-2 50-pin Ultra-Narrow single-ended
- 68-pin VHDI SCSI-3 Ultra2-Wide LVD
- Three Serial RS232C DB9 (local console, remote console, general purpose)
- Fast Ethernet RJ45
- Fast Ethernet RJ45 *Web Console*

3.37.4 Operating systems

- HP-UX: 64-bit 11.00, 11i v1 and 11i v2
- Linux

3.37.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
L3000-5Xrp2470	388	376	4.52-CPU: 8.94-CPU: 17.4	4.42-CPU: 8.34-CPU: 14.5
L3000-7Xrp2470	581		6.7 2-CPU: 12.9	

3.37.6 Dimensions

Model	**Height**	**Width**	**Depth**	**Weight**
	368mm	482mm	775mm	68kg
Rack-mounted	7U	482mm	775mm	68kg

3.37.7 References

Manuals

- User Guide rp5400 Family of Servers (URL gone)

Articles

- hp server rp5400 series entry-level UNIX servers technical whitepaper (URL gone)

3.38 HP N4000 (rp7400)

3.38.1 Overview

The HP 9000 rp7400 were mid-range PA-RISC servers and the original HP 9000 N-Class N4000 from the turn of the century. The original N4000 (rp7400) is based the Stretch system architecture, also used in the L1500 and L3000 (rp5430/rp5470) servers. Later rp7405 and rp7410 servers were also labeled N4000 and feature a similar set of I/O options and expandability in basically the same chassis, with a completely different system architecture, the Cell.

N4000s were shipped in two models with different system board, A3639A and A3639B. The N4000 that was later renamed to rp7400 was shipped with an even different mainboard and had the model number A3639C.

Model	rp	Product	Introduced	Price
N4000		A3639AA3639B	1999	$48,000
	rp7400	A3639B	2001	

The original N4000 (A3639A and A3639B) and later rp7400 (A3639C) are in fact different products, based on the same basic architecture but with slight differences, especially relating to the type and number of processors.

3.38.2 System

CPU

The rp7400 N4000 supports one to eight processors. Not all early N4000s support the later processors and a maximum number of CPUs.

Processor types are indicated with the following suffixes:

- -36: PA-8500 360 MHz with 512/1024 KB on-chip I/D L1 cache each [A3639A, A3639B, A3639C, A8327A]
- -44: PA-8500 440 MHz with 512/1024 KB on-chip I/D L1 cache each [A3639A, A3639B, A3639C, A8327A]
- -5X: PA-8600 550 MHz with 512/1024 KB on-chip I/D L1 cache each [A3639B, A3639C, A8327A]
- -6X: PA-8700 650 MHz with 768/1536 KB on-chip I/D L1 cache each [A3639C, A8327A]
- -7X: PA-8700 750 MHz with 768/1536 KB on-chip I/D L1 cache each [A3639C, A8327A]
- Itanium 2/IA64 processors were planned on the N4000 but apparently never offered.

Chipset

The rp7400 system is based on the Stretch chipset, used in the L1500 and L3000 (rp5430/rp5470) servers as well. Stretch has four main components:

1. Prelude memory controller, is the main crossbar of the system

2. Four DEW Runway converters, attach the processors to the main buses
3. Two IKE I/O controllers connect the PCI bridges via I/O channels
4. 14 Elroy PCI bridges (LBAs) convert the IKE I/O to PCI buses

The rest of the system is implemented with common parts:

- DEC 21142/43 Fast Ethernet controller
- Dual-channel Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controllers
- Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

The system bus architecture is interesting as it provides more bandwidth than could be used under practical circumstances. The designers probably counted on future CPU upgrades, such as Itanium processors.

- Two Itanium system buses, 133 MHz, each 2.1 GB/s peak, 4.3 GB/s aggregate
- Eight Runway+ CPU buses, each 2.1 GB/s peak, aggregate 17.0 GB/s
- Four Memory buses, each 2.1 GB/s peak, aggregate 8.5 GB/s
- 24 I/O channels, each 133 MHz 265 MB/s, aggregate 6.4 GB/s
- 14 PCI-64/66 I/O buses for expansion slots
- Three SCSI-3 Ultra2-Wide LVD main storage I/O buses, one for each internal drive and one for external devices

Memory

- ECC SDRAM DIMMs
- 16 slots
- 256 MB, 512 MB, 1 GB and 2 GB modules supported
- 32 GB maximum

Expansion

- Ten "Twin-Turbo" PCI 64-bit/66 MHz slots, each on an independent PCI bus, each connected via two I/O links/ropes (aggregate 530 MB/s), hot-plug capable
- Two "Turbo" PCI 64-bit/66 MHz slots, each on an independent PCI bus, each connected via one I/O link/rope (265 MB/s), hot-plug capable (one of these two Turbo slots is reserved for Core I/O LAN/SCSI)
- All slots keyed for 5.0 V (support either 5.0 V or universal PCI cards)

Drives

- Two internal Ultra SCSI LVD 3.5″ drives with SCA connector, hot-pluggable

3.38.3 External

- 68-pin VHDCI Ultra LVD external SCSI
- Three Serial RS232C DB9 (local console, remote console, general purpose) via a DB25 "M cable"
- 10/100 Mbit Ethernet TP/RJ45
- 10/100 Mbit Ethernet TP/RJ45 *LAN console*

3.38.4 Operating systems

- HP-UX: 64-bit 11.00, 11i v1, 11i v2 and 11i v3
- Linux

3.38.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
N4000-6X rp7400	493	489	5.7 2-CPU: 11.3 4-CPU: 22.1 8-CPU: 42.6	5.7 2-CPU: 10.4 4-CPU: 19.3 8-CPU: 30.5
N4000-7X rp7400	551	524	6.4 2-CPU: 12.5 4-CPU: 24.6 8-CPU: 46.7	6.1 2-CPU: 11.0 4-CPU: 20.5 8-CPU: 32.1

3.38.6 References

Manuals

- rp7400 Hardware Manual Hewlett-Packard Company (May 2002)
- hp server rp7400 system architecture and design guide, Hewlett-Packard Company (February 2002, product number 5981-0154EN) (URL gone)

3.39 HP N4000 (rp7405/rp7410)

3.39.1 Overview

The HP rp7405/rp7410 N4000 N-Class servers are up to 8-way multiprocessing servers and at the time smallest HP system which could be hardware-partitioned into logical servers, two **nPartitions**. Based upon the same 10U rack-mountable chassis as their rp7400/N4000 brethren, the newer rp7405 and rp7410 are built around a completely overhauled system and I/O architecture. The "Core Electronic Complex" is a modified version of the Superdome's cell-based system architecture, limited to two cells, which each contain up to four processors, sixteen memory slots and the central chipset.

The rp7405 was apparently an entry-level version of the rp7410 — based on the same hardware and with the same capabilities but shipped in smaller configurations. Upgrades to a "full" rp7410 were later possible, probably including a modified firmware for unlocking the full functionality.

Model	rp	Product	Introduced	Price
(N4000)	rp7405	A7111AA7112AA7113A	2002	$50,959
(N4000)	rp7410	A6752A	2002	$92,250

3.39.2 System

CPU

The rp7405 and rp7410 support from two to eight processors. They are based on different system boards with different model numbers.

- rp7405: A7111A (two-way), A7112A (four-way), A7113A (eight-way) support 650-750 MHz
- rp7410: A6752A support two to eight 650 MHz, 750 MHz and 875 MHz processors

Processor types are indicated with the following suffixes:

- -6X: PA-8700 650 MHz with 2.25MB L1 cache
- -7X: PA-8700 750 MHz with 2.25MB L1 cache
- -8X: PA-8700+ 875 MHz with 2.25MB L1 cache
- -9X: PA-8800 (dual-core) 900 MHz or 1.0 GHz with 3 MB on-chip L1 and 32 MB off-chip L2 cache
- Maybe: PA-8900 (dual-core) 800 MHz-1.1 GHz with 3 MB on-chip L1 and 64 MB off-chip L2
- Maybe: Itanium 2/IA64 processors are probably also possible on some models

Chipset

- Cell controller CC: the central chipset and crossbar. The CCs provide links for four processors, two memory banks, I/O via SBA, PDH and firmware, and second cell via the XBC.
- Master I/O controller SBA: located on the I/O backplane, each is linked to one cell Each SBA provides up to 32 links that connect to slave I/O controllers LBA.

  - 28 ropes link to 14 "Twin-Turbo" slots via 14 LBAs
  - Two ropes link to two "Turbo" PCI slots via two LBAs
  - Two links/ropes are connected via two LBAs to the Core I/O MP/SCSI cards
- Core I/O for the I/O functions system with a set of cards: MP/SCSI and LAN/SCSI.
  - Two dual-channel Symbios Logic 53C1010 Ultra160 SCSI controllers
  - Dual-channel Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller (MP/SCSI)
  - Gigabit Ethernet networking (LAN/SCSI)
  - Fast-Ethernet (DEC 21142/43) Management LAN (MP/SCSI)
  - The optional second Core I/O card set can be used for redundancy or partitioning
- 18 Elroy PCI bridges (**LBAs**) convert the links/ropes from the SBA into PCI bus (only 9 of these 18 LBAs are used when only one cell board is installed)

Buses

- Runway+/Runway DDR CPU bus, 125 MHz DDR, 64-bit, 2.0 GB/s per CPU, 16.0 GB/s max
- Memory bus 4.0 GB/s for each cell, aggregate 8.0 GB/s max
- XBC cell-to-cell link 8.0 GB/s aggregate
- SBA cell-to-I/O link 2.0 GB/s on each cell, aggregate 4.0 GB/s max
- 32 I/O links/ropes, 12-bit wide, 265 MB/s, 8.5 GB/s I/O peak
- 14 PCI-64/66 I/O buses for expansion slots
- Two PCI-64/33 I/O buses for expansion slots for Core I/O SCSI/LAN
- Two PCI-64/33 I/O buses for Core I/O MP/SCSI
- Two SCSI-3 Ultra160 LVD main storage I/O buses one on each cell
- Ultra SCSI SE for removable media

Memory

- ECC DIMMs, low-voltage TTL, 125 MHz frequency
- 256 MB, 512 MB and 1 GB modules supported
- 16 slots on each cell board
- 32 GB maximum, 64 GB with "future" memory modules

Expansion

There are up to 16 PCI 64-bit/66 MHz slots in the I/O cage, which can be fully accessed when using a system with two cells — with one cell board only seven slots are available. One PCI slot is dedicated to the Core I/O card set (see above) so only 15 of the 16 PCI slots are available for expansion options.

Drives

- Four trays for low-profile 3.5âĂș Ultra2-Wide LVD SCSI hard drives with 80-pin SCA connector, hot-plug
- One tray for a half-heigth 5.25âĂș 50-pin Ultra-Narrow SE SCSI drive, external accessible

3.39.3 External

- 68-pin VHDCI Ultra160 LVD external SCSI external channel from LAN/SCSI board
- Three Serial RS232C DB9 local console, remote console, UPS via a DB25 "M cable" on MP/SCSI board
- 10/100 Mbit Ethernet TP/RJ45 Management LAN on MP/SCSI board
- Gigabit Ethernet TP/RJ45 on LAN/SCSI board

3.39.4 Operating systems

- HP-UX: 64-bit (11.00,) 11i v1, 11i v2 and 11i v3

3.39.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
N4000-7Xrp7410			4-CPU: 25.38-CPU:49.9	4-CPU: 18.98-CPU:36.8

3.39.6 References

Manuals

- User Guide hp rp7405/7410 Servers (URL gone)
- hp server rp7410 whitepaper (URL gone)

3.40 HP 9000 rp3410 and rp3440

3.40.1 Overview

The HP 9000 rp3410 and rp3440 were some of the last PA-RISC-based HP servers, in a 2U rack-mountable case. They use dual-core PA-8800 or PA-8900 processors in a HP zx1 system design that was also used for Itanium 2 systems. There is an upgrade path to Intel/HP IA64 Itanium 2 processors. The HP 9000 rp4410 and rp4440 servers are technically similar with more computing and I/O possibilities.

rp	Introduced	Price
rp3410rp3410-2	2004	$4,000
rp3440rp3440-4	2004	$7,000

3.40.2 System

CPU

The rp3410 (rp3410-2) supports a single processor, the rp3440 (rp3440-4) up to 2-way multi-processing (SMP).

- rp3410:
  - 1 dual-core PA-8800 800 MHz with 3 MB L1 and 32 MB off-chip L2 cache
- rp3440:
  - 1 or 2 dual-core PA-8800 900 MHz-1.0 GHz with 3 MB L1 and 32 MB off-chip L2 cache
  - 1 or 2 dual-core PA-8900 800 MHz-1.1 GHz with 3 MB L1 and 64 MB off-chip L2 cache
- On some entry-level versions only one of the two CPU cores per processor is active
- An upgrade path to HP Itanium 2 processors was available

Chipset

The systems are based on HP's zx1 chipset, which consists of two main components, the MIO memory and I/O controller and the IOAs I/O adapters. The zx1 is almost a crossbar chipset: the zx1 memory controller acts as the crossbar switch which links processors, memory and I/O together.

- Pluto is the zx1 memory and I/O controller and connects the central system buses:
  1. Processor bus of 6.4 GB/s for one or two CPUs
  2. Two independent memory buses, each 4.25 GB/s
  3. I/O channels, six on rp3410 with 3.0 GB/s and eight on rp3440 with 4.0 GB/s

  The MIO also contains both memory and cache controllers.
- rp3410: Five Mercury I/O adapters IOAs for PCI-X slots
- >rp3440: Seven Mercury I/O adapters IOAs for PCI-X slots
- PCI-X slots and I/O channels:

1. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
2. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
3. *rp3440* PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
4. *rp3440* PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
5. Management LAN and serial ports (iLO card) on one channel — 0.5 GB/s
6. Ultra160 SCSI and Gigabit Ethernet controllers on one channel — 0.5 GB/s
7. IDE and USB controllers one channel — 0.5 GB/s

- Dual-channel Ultra160 SCSI controller, LSI Logic 53C1030
- Gigabit Ethernet controller, Broadcom Tigon 3
- IDE controller, PCI649
- USB2.0 controller

Buses

- Itanium 2/zx1 processor bus, 128-bit, 200 MHz, 6.4 GB/s
- Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s, aggregate 8.5 GB/s
- rp3410:
  - Six zx1 I/O channels/buses, aggregate 3.0 GB/s
  - Two PCI-X 64/133 I/O buses
- rp3440:
  - Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
  - Four PCI-X 64/133 I/O buses
- SCSI-3 Ultra160 LVD storage I/O bus
- IDE secondary storage I/O bus

Memory

- PC2100 DDR CL2 SDRAM DIMMs
- Twelve slots
- 1 GB minimum memory
- rp3410: 6 GB maximum memory
- rp3440: 32 GB maximum memory
- 8.5 GB/s memory bandwidth
- 80ns memory latency

Expansion

- One PCI-X 64-bit/133 MHz slot with 1 GB/s data rate
- rp3410: One PCI-X 64-bit/133 MHz slot with 512 MB/s data rate
- rp3440: Three PCI-X 64-bit/133 MHz slots with 512 MB/s data rate
- All PCI slots are 3.3 V

Drives

- Three 3.5âĂş Ultra160 LVD SCSI hard drives, 1âĂş height, 68-pin
- Slimline IDE CD or DVD drive

3.40.3 External

- Three Serial RS232C DB9 for local console, remote console, general purpose
- Four USB 2.0 ports
- TP/RJ45 Gigabit Ethernet
- HP Integrated Lights Out iLO system management card with Fast-Ethernet Web console
- Ultra160 SCSI 68-pin

3.40.4 Operating systems

- HP-UX11i v1, 11i v2, 11i v3
- Linux

3.40.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
rp3440 1.0 GHz dualcore			2-core: 18.7 2-CPU/4-core: 37.1	2-core: 19.2 2-CPU/4-core: 32.6

3.40.6 Dimensions

Model	**Height**	**Width**	**Depth**	**Weight**
Rack-mounted	2U	483mm	680mm	23kg
Stand-alone	495mm	295mm	675mm	26kg

3.40.7 References

Manuals

- User Service Guide HP 9000 rp3410 and HP 9000 rp3440 (.pdf) Hewlett-Packard Development Company (2010, sixth edition)
- Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers URL gone)

3.41 HP 9000 rp4410 and rp4440

3.41.1 Overview

The HP 9000 rp4410 and rp4440 were, like the HP 9000 rp3410 and rp3440, some of the last PA-RISC-based HP servers, based on up to four dual-core PA-8800 or PA-8900 processors and HP zx1 chipset, technically very similar to the rp3400s. The systems can be rack-mounted in 4U or be used stand-alone.

rp	Introduced	Price
rp4410rp4410-4	2004	
rp4440rp4440-8	2004	$21,000

3.41.2 System

CPU

The rp4410 (rp4410-4) supports 2-way multi-processing (SMP), the rp4440 (rp4440-8) up to 4-way multi-processing (SMP).

- Dual-core PA-8800 900 MHz-1.0 GHz with 3 MB on-chip L1 and 32 MB off-chip L2 cache
- Dual-core PA-8900 800 MHz-1.1 GHz with 3 MB on-chip L1 and 64 MB off-chip L2 cache
- There probably was an upgrade path to Itanium 2/IA64 processors.

Chipset

The systems are based on the HP zx1 chipset with three main components — the MIO memory and I/O controller, the IOAs I/O adapters and the SMEs scalable memory expanders.

- Pluto is the zx1 MIO memory and I/O controller and connects the system buses:
  1. Processor bus of 6.4 GB/s for one or two dual-CPU modules
  2. Two independent memory buses with each 6.4 GB/s
  3. Eight I/O channels with aggregate 4.0 GB/s
- Six zx1 SMEs scalable memory expanders attach to two independent zx1 memory buses
- Six Mercury zx1 IOAs I/O adapters connect the PCI-X slots
  1. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
  2. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
  3. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
  4. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
  5. Core I/O adapters like SCSI, Ethernet etc. on two channels — 1.0 GB/s
- Dual-channel Ultra320 SCSI controller
- Dual-port Gigabit Ethernet

- USB2.0 controller
- IDE controller

Buses

An interesting aspect of the rp4400's bus setup is that the same 6.4 GB/s processor bus is shared between up to two CPUs on the rp4410 and up to four CPUs on the rp4440.

- Itanium 2/zx1 processor bus 6.4 GB/s
- Two independent zx1 memory buses, 200 MHz, each 6.4 GB/s
- Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
- Two PCI-X 64/133 I/O buses
- Two PCI-X 64/66 I/O buses
- SCSI-3 Ultra320 LVD storage I/O bus
- IDE secondary storage I/O bus

Memory

- PC2100 parity ECC DDR CL2 SDRAM DIMMs
- 16- or 32-DIMM carrier board
- 1 GB minimum memory
- 128 GB maximum memory
- 12.8 GB/s memory bandwidth
- 105ns memory latency

Expansion

- Two PCI-X 64-bit/133 MHz slots, each on an independent bus, hot-plug
- Four PCI-X 64-bit/66 MHz slots, on two shared buses, hot-plug
- All PCI slots are 3.3 V

Drives

- Two bays for 3.5âĂş Ultra320 LVD SCSI hard drives, hot-plug
- Slimline bay for optional IDE CD or DVD drive

3.41.3 External

- Three Serial RS232C DB9 for local console, remote console, general purpose
- Two USB 2.0 ports
- Two Gigabit Ethernet, TP/RJ45
- Two Ultra320 SCSI ports
- HP Integrated Lights Out iLO system management card with Fast-Ethernet Web console

3.41.4 Operating systems

- HP-UX11i v1, 11i v2, 11i v3
- Linux could be a possibility, as the similar rp3400s are supported, albeit unofficially

3.41.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
rp4440 1.0 GHz dualcore			2-core: 18.6 2-CPU/4-core: 37.0 4-CPU/8-core: 73.2	2-core: 19.3 2-CPU/4-core: 34.7 4-CPU/8-core: 55.4

3.41.6 Dimensions

Model	**Height**	**Width**	**Depth**	**Weight**
Rack-mounted	4U	440mm	690mm	53kg
Stand-alone	530mm	261mm	695mm	53kg

3.41.7 References

Manuals

- User Service Guide HP 9000 rp4410 and HP 9000 rp4440 (.pdf, 17 MB) Hewlett-Packard Development Company (2009, fifth edition)
- Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers (URL gone)

3.42 HP Integrity rx1600 and rx1620

3.42.1 Overview

The rx1600 (later rx1600-2) is a 1U rack-mountable server with up to two Itanium 2 Deerfield processors. The later introduced rx1620 supported newer Fanwood Itanium 2 processors. Both classes of CPUs are specified/marketed as "low-voltage."

3.42.2 System

CPU

rx1600/rx1600-2

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 *Deerfield*low-voltage	1.0 GHz	16/16 KB	256 KB	1.5 MB

rx1620

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 *Fanwood*low-voltage	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-2	Itanium 2 *Fanwood*low-voltage	1.6 GHz	16/16 KB	256 KB	3.0 MB

All caches are on-die (L1, L2 and L3).

Chipset

The systems are based on the HP zx1 chipset with two central components — Pluto and Mercury.

- Pluto: main chipset controller connects to three system buses:
  1. Processor bus
  2. Two independent memory buses
  3. Seven I/O channels

  It contains both memory and cache controllers as well.
- Five Mercury I/O adapters: connect PCI-X slots and I/O devices to Mercury
  1. PCI-X 64/133 slot on two channels with 1.0 GB/s
  2. PCI-X 64/133 slot on two channels with 1.0 GB/s
  3. Gigabit Ethernet and Ultra320 SCSI (Core I/O) on PCI on one channel with 0.5 GB/s
  4. IDE, USB, Fast-Ethernet LAN (Core I/O) on PCI on one channel with 0.5 GB/s
  5. Management Ethernet LAN, VGA, serial (Core I/O) on PCI on one channel with 0.5 GB/s

The remained consists of standard third-party I/O chipsets:

- Gigabit Ethernet (Broadcom 5701)

- rx1600: Fast Ethernet
- Two-channel Ultra320 SCSI controller (LSI 53C1030)
- Ultra ATA-100 IDE controller (PCI649)
- Serial controller, DUART (16550A-compatible)
- 10/100 Ethernet for management (Intel 82550)
- Management processor card included by default
- Processor Dependent Hardware (PDH) Controller
- FPGA controller for ACPI (2.0) and LPC
- Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)
- EHCI USB controller

Buses

- Itanium 2/zx1 processor bus — 200 MHz DDR with 6.4 GB/s bandwidth on 1.0 and 1.3 GHz processors, 266 MHz DDR with 8.5 GB/s on 1.6 GHz processors (rx1620)
- Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s — aggregate 8.5 GB/s memory bandwidth
- Seven zx1 I/O channels/buses, aggregate 3.5 GB/s
- Four PCI-X 64/133 I/O buses for expansion cards
- Three PCI-X 64/133 I/O buses for Core I/O cards (SCSI, networking, etc.)
- Two SCSI-3 Ultra320 (LVD) storage I/O buses
- UltraATA-100 IDE storage I/O bus

Memory

- PC2100 ECC DDR CL2 SDRAM DIMMs
- Takes up to 2 GB modules
- Eight slots
- DIMMs must be installed in quads
- 1 GB minimum (4×256 MB)
- 16 GB maximum (8×2 GB)
- 8.5 GB/s memory bandwidth

Expansion

- PCI-X 64-bit/133 MHz slot, full-length
- PCI-X 64-bit/133 MHz slot, half-length
- All PCI slots are 3.3 V

Drives

- Two internal 3.5âĂş bays for 1âĂş height Ultra320 SCSI SCA 80-pin hard drives, hot-plug;
- Slimline bay for optional IDE CD or DVD drive

3.42.3 External

- Gigabit Ethernet, TP/RJ45
- rx1600: 10/100 Ethernet, TP/RJ45
- rx1620: Second Gigabit Ethernet, TP/RJ45
- 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- VGA graphics
- Ultra320 SCSI 68-pin HDCI
- 25-pin serial for management processor card, needs break-out cable for three serial ports
- Two USB 2.0 ports
- Two Serial RS232C DB9

3.42.4 Operating systems

- HP-UX: 11i v1, 11i v2 and 11i v3
- Linux for Itanium
- Windows Server 2003 64-bit
- OpenVMS

3.42.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000*rate*, int**	**SPEC2000*rate*, fp**
rx1600 1.0 GHz 1.5 MB	837	1382	9.71 2-CPU: 19.1	16.0 2-CPU: 27.6
rx1620-21.3 GHz 3.0 MB	1178	2214	13.7 2-CPU: 27.0	25.7 2-CPU: 42.7
rx1620-21.6 GHz 3.0 MB	1452	2692	16.8 2-CPU: 33.2	31.2 2-CPU: 50.4

3.42.6 References

Manuals

- HP Integrity rx1600 Operation and Maintenance (PDF) Hewlett-Packard Development Company (2010)
- HP Integrity rx1620 Operations Guide (PDF) Hewlett-Packard Development Company (2012)
- HP Integrity rx1620 Maintenance Guide (PDF) Hewlett-Packard Development Company (2012)
- Overview of the HP Integrity rx1600, rx2600, rx4640, and rx5670 servers technical whitepaper (URL gone)
- Overview of the HP Integrity rx1620, rx2620, and rx4640 Servers (URL gone)

3.42.7 Dimensions

Height	Width	Depth	Weight
1U	482mm	680mm	22kg

3.43 HP Integrity rx2600 and rx2620

3.43.1 Overview

The rx2600 is a rack-mountable HP Itanium workstation based on the zx6000 workstation. Both have a similar system design and can be mounted in 2U in 19″ racks. The rx2600 supports up to two Itanium 2 processors and is targeted for PCI-X devices and thus does not feature the AGP port of the workstation-oriented zx6000.

The rx2600 was later marketed as **rx2600-2**.

3.43.2 System

CPU

rx2600/rx2600-2

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 *Deerfield*?low-voltage	1.0 GHz	16/16 KB	256 KB	1.5 MB
1-2	Itanium 2 *Madison*	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-2	Itanium 2 *Madison*	1.4 GHz	16/16 KB	256 KB	1.5 MB
1-2	Itanium 2 *Madison*	1.5 GHz	16/16 KB	256 KB	6.0 MB

rx2620

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 *Madison?*	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-2	Itanium 2 *Madison?*	1.6 GHz	16/16 KB	256 KB	3.0 MB
1-2	Itanium 2 *Montecito*dual-core	1.4 GHz	16/16 KB	1024/256 KB	12 MB
1-2	Itanium 2 *Montecito*dual-core	1.6 GHz	16/16 KB	1024/256 KB	18 MB

All caches are on-die (L1, L2 and L3).

Chipset

The systems are based on HP's **zx1 chipset**, which consists of two main components — the **MIO** (memory and I/O controller) and the **IOAs** (I/O adapters):

- Pluto zx1 MIO (memory and I/O controller) is the main chipset controller and connects the three central system buses:
  1. Processor bus (6.4 GB/s at 200 MHz DDR)
  2. Two independent memory buses (each 4.25 GB/s)
  3. Eight I/O channels (aggregate 4.0 GB/s, via the IOAs, see below)

  The zx1 MIO also contains both memory and cache controllers.
- Seven Mercury zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 4.0 GB/s on eight 0.5 GB/s channels

1. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
2. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
3. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
4. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
5. Core I/O: IDE, USB, serial, (rx2600 only: Fast-Ethernet LAN) in a PCI 64/133 slot on one channel — 0.5 GB/s
6. Core I/O: Gigabit Ethernet and Ultra320 SCSI (on rx2620 there are each two Gigabit Ethernet and SCSI controllers) in a PCI 64/133 slot on one channel — 0.5 GB/s
7. Management: Ethernet LAN, VGA, serial in a PCI 64/133 slot on one channel — 0.5 GB/s

The rest are standard third-party I/O chips:

- Gigabit Ethernet (Broadcom 5701)
- Two-channel Ultra320 SCSI controller (LSI 53C1030)
- Ultra ATA-100 IDE controller (PCI649)
- Serial controller, DUART (16550A-compatible)
- 10/100 Ethernet for management (Intel 82550)
- Management processor card included by default ("ECI card") — includes serial/ remote management and VGA
- Radeon VGA graphics
- EHCI USB controller
- Processor Dependent Hardware (PDH) Controller
- FPGA controller for ACPI (2.0) and LPC
- Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)

Buses

- Itanium 2/zx1 processor bus 6.4 GB/s at 200 MHz DDR
- Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s — aggregate 8.5 GB/s memory bandwidth
- Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
- Four PCI-X 64/133 I/O buses for expansion cards
- Three PCI-X 64/133 I/O buses for Core I/O cards (SCSI, networking, etc.)
- Two SCSI-3 Ultra320 (LVD) storage I/O buses
- UltraATA-100 IDE storage I/O bus

Memory

- PC2100 ECC DDR CL2 SDRAM DIMMs
- rx2600: up to 2 GB modules
- rx2620: up to 4 GB modules
- Twelve slots
- DIMMs must be installed in quads
- 1 GB minimum (4×256 MB)
- rx2600: 24 GB maximum (12×2 GB)
- rx2620: 32 GB maximum (8×4 GB — the remaining four slots cannot be used)
- 8.5 GB/s memory bandwidth

Expansion

- Four PCI-X 64-bit/133 MHz slots, full-length
- All PCI slots are 3.3 V

Drives

- Three internal 3.5âĂș bays for Ultra320 SCSI SCA 80-pin hard drives, hot-plug; drives 1 and 2 are on one SCSI channel, drive 3 on the second SCSI channel
- Slimline bay for optional IDE CD or DVD drive

3.43.3 External

- rx2600: Gigabit Ethernet, TP/RJ45
- rx2620: Dual-Port Gigabit Ethernet, TP/RJ45
- 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- VGA graphics
- Ultra320 SCSI 68-pin
- 25-pin serial for management processor card, needs break-out cable for three serial ports
- Four USB 2.0 ports
- Two Serial RS232C DB9

3.43.4 Operating systems

- rx2600: HP-UX11i v1.6, 11i v2 and 11i v3
- rx2620: HP-UX11i v2 and 11i v3

- Linux for Itanium
- Windows Server 2003 64-bit
- OpenVMS

3.43.5 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000*rate*, int	SPEC2000*rate*, fp
rx2600900 MHz 1.5 MB	674	1151	7.8 2-CPU: 15.5	2-CPU:
rx2600 1.0 GHz 3.0 MB	810	1427	9.4 2-CPU: 18.7	2-CPU:
rx2600 1.3 GHz 3.0 MB	1073	1808	12.4 2-CPU: 24.8	2-CPU:
rx2600 1.5 GHz 6.0 MB	1408	2119	15.3 2-CPU: 30.5	2-CPU:
rx2620-2 1.3Hz 3.0 MB	1170	2229	13.6 2-CPU: 26.9	15.9 2-CPU: 27.7
rx2620-2 1.6Hz 3.0 MB	1408	2553	16.3 2-CPU: 32.3	29.6 2-CPU: 48.5
rx2620-2 1.6Hz 6.0 MB	1535	2675	17.8 2-CPU: 35.5	31.0 2-CPU: 51.5

3.43.6 Dimensions

Model	Height	Width	Depth	Weight
Tower	495mm	297mm	673mm	25kg
Rack-mounted	2U	482mm	680mm	22kg

3.43.7 References

Manuals

- Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000 (PDF) Hewlett-Packard Development Company (September 2003, second edition)
- HPE Integrity rx2620 Server User Service Guide (PDF) Hewlett-Packard Enterprise (2015)
- Overview of the HP Integrity rx1620, rx2620, and rx4640 Servers (URL gone)
- Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper (URL gone)

3.44 HP Integrity rx4610

3.44.1 Overview

The Integrity rx4610 were HP's first-generation Itanium servers based on up to four *Merced* Itanium processors in an 7U rack-mountable case. The rx4610 offered many I/O and expansion options with ten PCI slots on four PCI buses (attached to 2.1 GB/s I/O bandwidth) and up to 64 GB of main memory but was limited to only two internal SCSI drives.

The rx4610 is based on the Intel Itanium reference architecture — the 82460GX chipset, which looks like a mix of PC-style (Frontside Bus to the processor) and PA-RISC (I/O "ropes" from the central chipset to PCI converters) platforms. The other HP system with Merced processors and the 82460GX was the HP i2000 workstation. Both the i2000 and rx4610 were rather slow and buggy when compared to contemporary PA-RISC systems.

3.44.2 System

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
2-4	Itanium 1 *Merced*	733 MHz	16/16 KB	96 KB	2.0 MB
2-4	Itanium 1 *Merced*	800 MHz	16/16 KB	96 KB	4.0 MB

L1 and L2 caches are on-die, L3 is off-chip

Chipset

The rx4610 is based on Intel's **82460GX** chipset with four main components:

1. **82460GX SAC** (System Address Chip) is the central chipset part:
   - ◈ System bus (FSB) for up to four processors — 2.1 GB/s (the SAC connects to the address and control parts of the FSB)
   - ◈ Four I/O channels to which the PCI buses attach (via the WXBs/PXB) — each channel is 533 MB/s
   - ◈ Connection to the SDC
   - ◈ Address/control access to the main memory
2. Three **82460GX WXBs** (Wide eXpansion Bridges) which connect the PCI 64/66 buses via three I/O channels to the SAC
   - ◈ One I/O channel connects to two PCI 64/66 slots
   - ◈ One I/O channel connects to three PCI 64/66 slots
   - ◈ One I/O channel connects to three PCI 64/66 slots and the SCSI controller
3. **82460GX PXB** (PCI eXpansion Bridge) connects the PCI 64/33 bus and core I/O (Ethernet LAN, PS/2, parallel, serial, IDE, USB, VGA) and the baseboard management controller via one I/O channel to the SAC

4. **82460GX SDC** (System Data Chip) is the central memory data controller:
    - ◈ It connects to the data part of the FSB system main bus
    - ◈ Has a private link to the SAC (PD)
    - ◈ Connects to the memory subsystem (data transfers, in contrast to the SAC's Address/control access)

The rest of the chipset is made up of standard (third-party) I/O components:

- ◈ Dual-channel Ultra3 SCSI controller
- ◈ Intel 82559 Fast Ethernet controller
- ◈ ATI Rage 128VR 64-bit SVGA with 16 MB video memory
- ◈ Baseboard management controller (BMC) for IPMI, EMP and WoL
- ◈ I/O and Firmware Bridge (IFB) communicates to IDE, USB and Super I/O
- ◈ ATA-33 IDE controller (on IFB)
- ◈ USB controller (on IFB)
- ◈ LPC47B27 Super I/O (serial and PS/2 ports controller)

Buses

- ◈ System bus, 32bit 133 MHz DDR ("double-pumped"), 2.1 GB/s, ECC-protected
- ◈ Memory bus, 266 MHz, 4.2 GB/s peak
- ◈ 2.1 GB/s aggregate I/O bandwidth with four 533 MB/s I/O channels
- ◈ Three PCI 64/66 I/O buses for expansion slots
- ◈ PCI 64/33 I/O bus for expansion slots and onboard devices

Memory

- ◈ Two memory boards, each supports up to 32 GB of memory
- ◈ 72-bit DIMMs
- ◈ 32 slots on each memory board
- ◈ Up to 1 GB modules
- ◈ 1 GB minimum (*i.e.,* one board)
- ◈ 64 GB maximum (64×1 GB — 32 modules on two boards)

Expansion

- ◈ Eight PCI 64-bit/66 MHz slots, full-length, hot-plug, 3.3 V
    - – Two slots are on one I/O channel

- Three slots are on one I/O channel
- Three slots are on one I/O channel which is shared with the SCSI subsystem

◈ Two PCI 64-bit/33 MHz slots, full-length, 5.0 V

Drives

◈ Two internal 3.5âĂş bays for 1âĂş height LVD SCA2 SCSI hard drives

◈ Optional IDE DVD drive in 0.5âĂş carrier

◈ Optional IDE floppy drive (LS120) in 0.5âĂş carrier

3.44.3 External

◈ 10/100 Ethernet, TP/RJ45

◈ VGA graphics

◈ External SCSI

◈ Two PS/2 for keyboard and mouse

◈ Parallel port

◈ Two 9-pin serial

◈ Two USB

3.44.4 Operating systems

◈ HP-UX11i v1.5,

◈ Linux for Itanium

◈ Windows 64-bit

3.44.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000*rate*, int**	**SPEC2000 *rate*, fp**
rx4610733 MHz 2 MB		625		7.22-CPU: 12.74-CPU: 20.1
rx4610800 MHz 4 MB	379	701	4.4	8.12-CPU: 14.24-CPU: 22.4

3.44.6 Dimensions

Height	**Width**	**Depth**	**Weight**
7U	444mm	711mm	68kg

3.44.7 References

Manuals

- hp server rx4610 User Guide (URL gone)
- An overview of the Itanium-based hp rx4610 server whitepaper (URL gone)

3.45 HP Integrity rx4640

3.45.1 Overview

The Integrity rx4640 (rx4640-8) are second-generation Itanium servers from HP with up to four Itanium 2 processors in a 4U rack-mountable case. In contrast to the rx4610 predecessors (7U, first-generation Itanium) the rx4640 is a completely new design based on the HP zx1 Itanium chipset, with double the I/O bandwidth and three times the processor and memory bandwidth. The rx4640 features a large amount of maximum memory (128 GB) but fewer PCI slots (six) and only the same small number of two internal SCSI drives.

The rx4640 was later marketed as **rx4640-8**.

3.45.2 System

CPU

The "standard" rx4640 supported out of the box up to four Itanium 2 processors:

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3	Other
1-4	Itanium 2 *Madison*	1.3 GHz	16/16 KB	256 KB	3.0 MB	
1-4	Itanium 2 *Madison*	1.5 GHz	16/16 KB	256 KB	6.0 MB	

Later rx4640 models (probably with a firmware upgrade) supported various newer processors, including dual-core Montvale CPUs and the **mx2** dual-CPU modules.

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3	Other
1-4	Itanium 2 *Madison*	1.6 GHz	16/16 KB	256 KB	6.0 MB	
1-4	Itanium 2 *Madison*	1.6 GHz	16/16 KB	256 KB	9.0 MB	
1-4	Itanium 2 *Montvale* dual-core (9140N)	1.6 GHz	16/16 KB	1024/256 KB	18 MB	
1-4	Itanium 2 *Montvale* dual-core (9150N)	1.6 GHz	16/16 KB	1024/256 KB	24 MB	
1-4	Itanium 2 mx2 *Hondo*dual-CPU module	1.1 GHz	16/16 KB	256 KB	4.0 MB	32 MB L4

Chipset

The rx4640 are based on HP's **zx1 chipset**, which consists of three main components — the **MIO** (memory and I/O controller), the **IOAs** (I/O adapters) and the **SMEs** (scalable memory expanders):

- Pluto zx1 MIO (memory and I/O controller) is the main chipset controller and connects the three central system buses:
  1. Processor bus (6.4 GB/s at 200 MHz DDR)
  2. Two independent memory buses (each 6.4 GB/s)
  3. Eight I/O channels (aggregate 4.0 GB/s, via the IOAs, see below)

  The zx1 MIO also contains both memory and cache controllers.
- Six zx1 SMEs (scalable memory expanders) attach to two independent zx1 memory buses (each 6.4 GB/s with three SMEs)

- Six Mercury zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 4.0 GB/s on eight 0.5 GB/s channels
  1. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
  2. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
  3. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
  4. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
  5. Core I/O: SCSI and Gigabit Ethernet on one channel — 0.5 GB/s
  6. Core I/O: Management LAN, IDE, USB, serial and VGA on one channel — 0.5 GB/s

The rest are standard third-party I/O chips:

- Gigabit Ethernet (Broadcom 5701)
- Two-channel Ultra320 SCSI controller (LSI 53C1030)
- Ultra ATA-100 IDE controller (PCI649)
- EHCI USB controller
- Serial controller, DUART (16550A-compatible)
- "Diva" remote management processor — serial and LAN
- Processor Dependent Hardware (PDH) Controller
- FPGA controller for ACPI (2.0) and LPC
- Baseboard Management Controller for IPMI management interface (the BMC is a ARM7 RISC processor)

Buses

- Itanium 2/zx1 processor bus 6.4 GB/s at 200 MHz DDR
- Two independent zx1 memory buses, 200 MHz, each 6.4 GB/s — aggregate 12.8 GB/s memory bandwidth
- Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
- Two PCI-X 64/133 I/O buses
- Two PCI-X 64/66 I/O buses
- PCI-X 64/66 I/O bus (for SCSI/Gigabit Ethernet onboard)
- PCI 32/33 I/O bus (for IDE/USB/management onboard devices)
- Two SCSI-3 Ultra320 (LVD) storage I/O buses
- UltraATA-100 IDE storage I/O bus

Memory

- DDR200 CL2 registered ECC SDRAM DIMMs, 200 MHz, 184-pin 2.5 V
- Takes up to 4 GB modules
- 16-DIMM or 32-DIMM memory carrier board
- DIMMs must be installed in quads
- 1 GB minimum (4×256 MB)
- 64 GB maximum with 16-DIMM board (16×2 GB), 128 GB maximum with 32-DIMM board (32×4 GB)
- 12.8 GB/s memory bandwidth

Expansion

- Four PCI-X 64-bit/66 MHz slots, hot-plug. 3.3 V
- Two PCI-X 64-bit/133 MHz slots, hot-plug. 3.3 V

Drives

- Two internal 3.5âĂș bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug; each drive can be configured on one separate channel — if they are on the same channel the second can be used for external SCSI devices
- Slimline bay for optional IDE CD or DVD drive

3.45.3 External

- Dual-port Gigabit Ethernet, TP/RJ45
- 10/100 Ethernet, TP/RJ45 management network (on management processor card)
- VGA graphics
- Two external Ultra320 SCSI 68-pin
- 25-pin serial for management processor card, needs break-out cable for three serial ports
- Four USB 2.0 ports
- Two (three?) Serial RS232C DB9

3.45.4 Operating systems

- HP-UX11i v2 and 11i v3
- Linux for Itanium
- Windows Server 2003 64-bit
- OpenVMS

3.45.5 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000 *rate*, int	SPEC2000 *rate*, fp
rx4640 1.3 GHz 3.0 MB	1132	1891	13.1 2-CPU: 25.8 4-CPU: 51.4	21.9 2-CPU: 37.9 4-CPU: 57.4
rx4640 1.5 GHz 6.0 MB	1404	2161	16.3 2-CPU: 32.5 4-CPU: 64.2	25.1 2-CPU: 43.2 4-CPU: 65.6
rx4640-8 1.5 GHz 4.0? MB	1372	2502	15.9 2-CPU: 31.7 4-CPU: 62.2	29 2-CPU: 48.3 4-CPU: 70.5
rx4640-8 1.6 GHz 9 MB	1590	2712	4-CPU: 72.5	4-CPU: 77.9

3.45.6 Dimensions

Height	Width	Depth	Weight
4U	482mm	690mm	45kg

3.45.7 References

Manuals

- User Service Guide HP Integrity rx4640 Server (URL gone)
- Overview of the HP Integrity rx1600-2, rx2600-2, and rx4640-8 servers technical whitepaper (URL gone)
- Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper (URL gone)

3.46 HP Integrity rx5670

3.46.1 Overview

The HP Integrity rx5670 are rack-mountable multi-processor Itanium 2 servers with up to four processors. Closely matching the rx4640 system architecture, the rx5670 is based on HP's zx1 Itanium chipset. PA-RISC L-Class servers (built into the same system/chassis) could be upgraded by a "board-swap" — changing the main system board, processors and support hardware — to Itanium 2 rx5670s (applies to HP rp5400/rp5450 (L1000/L2000) and HP rp5430/rp5470 (L1500/L3000)).

3.46.2 System

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-4	Itanium 2 *Madison*	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-4	Itanium 2 *Madison*	1.3 GHz	16/16 KB	256 KB	6.0 MB

All caches are on-die (L1, L2 and L3).

Chipset

The rx5670 is based on HP's **zx1 chipset**, which consists of three main components — the **MIO** (memory and I/O controller), the **IOAs** (I/O adapters) and the **SMEs** (scalable memory expanders):

- Pluto zx1 MIO (memory and I/O controller) is the main chipset controller and connects the three central system buses:
  1. Processor bus (6.4 GB/s at 200 MHz DDR)
  2. Two independent memory buses (each 6.4 GB/s with six SMEs)
  3. Eight I/O channels (aggregate 4.0 GB/s, via the IOAs, see below)

  The zx1 MIO also contains both memory and cache controllers.
- Twelve zx1 SMEs (scalable memory expanders), six on each DIMM/memory carrier board, attach to two independent zx1 memory buses (each 6.4 GB/s)
- Eight Mercury zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 4.0 GB/s on eight 0.5 GB/s channels
  1. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
  2. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
  3. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
  4. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
  5. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
  6. Two PCI-X 64/66 I/O slots on one channel — 0.5 GB/s

7. One PCI 64/66 slot for Gigabit Ethernet and one SCSI controller (Core I/O) on one channel — 0.5 GB/s
8. One PCI 64/66 slot for management LAN, serial and one SCSI controller (Core I/O); and one PCI 64/33 slot for optional graphics/USB on one channel (with the other slot) — 0.5 GB/s

The rest are standard third-party I/O chips, implemented on Core I/O cards in two or three PCI slots

- Dual-channel Ultra160 SCSI controllers (LSI 53C1010)
- SCSI controller (LSI 53C896)
- Gigabit Ethernet (Broadcom 5701)
- Serial controller, DUART (16550A-compatible)
- IBM PCI-X to PCI-X bridge
- "Diva" remote management processor — serial and LAN
- Optional Radeon VGA graphics (with USB on one card)
- Optional EHCI USB controller

Buses

- Itanium 2/zx1 processor bus 6.4 GB/s at 200 MHz DDR
- Two independent zx1 memory buses, 266 MHz, each 6.4 GB/s — aggregate 12.8 GB/s memory bandwidth
- Eight zx1 I/O channels/buses, aggregate 4.0 GB/s
- Three PCI-X 64/133 I/O buses for expansions slots
- Three PCI-X 64/66 I/O buses for expansion slots
- PCI-X 64/66 I/O bus for Core I/O expansion slots
- PCI 64/33 I/O bus for graphics/USB slot
- Two SCSI-3 Ultra160 (LVD) storage I/O buses

Memory

- PC2100 ECC DDR CL2 SDRAM DIMMs
- Takes up to 2 GB modules
- One or two 24-DIMM memory carrier boards
- DIMMs must be installed in quads
- 1 GB minimum (4×256 MB)
- 96 GB maximum with two 24-DIMM boards (48×2 GB)
- 12.8 GB/s memory bandwidth

Expansion

- Three PCI-X 64-bit/133 MHz slots
- Six PCI-X 64-bit/66 MHz slots
- Two PCI slots preloaded with core I/O cards
- One PCI 64/33 MHz slot for graphics/USB card (optional)

Drives

- Four internal 3.5âĂș bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug, each pair of drives is connected to one separate controller and each drive in each pair is on a seperate channel
- One open bay for removable SCSI media drives — DVD/DDS

3.46.3 External

- Gigabit Ethernet, TP/RJ45
- 10/100 Ethernet, TP/RJ45 management network with web console (on management processor card)
- Ultra160 SCSI 68-pin
- Three Serial RS232C DB9 (console, remote console, general purpose)
- Four USB 2.0 ports (optional)
- VGA graphics (optional)

3.46.4 Operating systems

- HP-UX11i v1.6, 11i v2 and 11i v3
- Linux for Itanium
- Windows Server 2003 64-bit
- OpenVMS

3.46.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000 *rate*, int**	**SPEC2000 *rate*, fp**
rx5670 900 MHz 1.5 MB	673	1151	7.81 2-CPU: 15.5 4-CPU: 30.4	13.3 2-CPU: 24.5 4-CPU: 38.7
rx5670 1.0 GHz 3.0 MB	807	1431	9.36 2-CPU: 18.6 4-CPU: 36.8	16.6 2-CPU: 30.7 4-CPU: 49.3

rx5670 1.3 GHz 3.0 MB	1066	1814	12.4 2-CPU: 24.5 4-CPU: 48.6	21.0 2-CPU: 37.3 4-CPU: 57.2
rx5670 1.5 GHz 6.0 MB	1312	2108	15.2 2-CPU: 30.3 4-CPU: 60.0	24.5 2-CPU: 42.6 4-CPU: 66.4

3.46.6 Dimensions

Height	Width	Depth	Weight
7U	482mm	740mm	72kg

3.46.7 References

Articles

- Overview of the HP Integrity rx2600, rx4640, and rx5670 servers technical whitepaper (PDF) Hewlett-Packard Development Company (October 2003, first edition, 5982-1595EN)

3.47 Convex Exemplar SPP1000, SPP1200 & SPP1600

3.47.1 Overview

The Convex Exemplar SPP1000, SPP1200 and SPP1600 are scalable 32-bit mainframe computing systems, with either PA-7100 or PA-7200 processors. Previous Convex designs used custom Convex processors, with SPP Convex switched to HP PA-RISC designs. At the same time, Convex and HP started collaborating more closely in the early 1990s, which resulted in the joint HP/Convex Exemplar SPP2000, and the takeover of Convex by HP in 1994. This development peaked with the HP-branded V-Class servers based on similar architecture, the 64-bit non-clusterable HP 9000/V2200 and V2250 and the up to four-way clusterable HP 9000/V2500 and V2600.

The 32-bit Convex SPP1x00 systems consist of three distinct system types, the **CD** compact systems, the **XA** eXtended Architecture hypernodes and the **XA** clusters:

- **SPP1000/CD, SPP1200/CD, SPP1600/CD**: single "compact" systems, either special systems with up to sixteen processors, or two SPP XA Hypernodes coupled together and sold as a single, non-clusterable system.
- **SPP1000/XA, SPP1200/XA, SPP1600/XA Hypernode**: a single XA hypernode with up to eight processors and provisions for linking up via SCI to other systems.
- **SPP1000/XA, SPP1200/XA, SPP1600/XA Cluster**: up to sixteen XA hypernodes coupled via SCI/TCI interconnection rings; these XA clusters can have up to 128 processors in their maximum configuration. The resulting interconnected Exemplars are ccNUMA computers.

The internal Exemplar architecture is based on a 5x5 crossbar with the central internal "switching" component, the crossbar, connecting the resources to each other by forming matrix connections between the devices' input and output ports. "5x5" because the crossbar has five ports for processors, memory and I/O.

The Nodes and Clusters are controlled and booted via a separate workstation connected to it, frequently a IBM RS/6000 computer running AIX, which faced the Exemplar's console and control I/O, in the case of a cluster only one node had a control workstation. Also apparently used were HP 9000/715 workstations running as "teststation."

3.47.2 System

CPU

- SPP1000/CD: 2-16 PA-7100 100 MHz with 2 MB off-chip L1 cache each
- SPP1000/XA Hypernode: 2-8 PA-7100 100 MHz with 2 MB off-chip L1 cache each
- SPP1000/XA Cluster: 8-128 PA-7100 100 MHz with 2 MB off-chip L1 cache each
- SPP1200/CD: 2-16 PA-7200 120 MHz with 512 KB off-chip L1 cache each
- SPP1200/XA Hypernode: 2-8 PA-7200 120 MHz with 512 KB off-chip L1 cache each
- SPP1200/XA Cluster: 8-128 PA-7200 120 MHz with 512 KB off-chip L1 cache each
- SPP1600/CD: 2-16 PA-7200 120 MHz with 1 MB off-chip L1 cache each
- SPP1600/XA HyperNode: 2-16 PA-7200 120 MHz with 1 MB off-chip L1 cache each

- ◈ SPP1600/XA Cluster: 8-128 PA-7200 120 MHz with 1 MB off-chip L1 cache each

It is not quite clear how the CD models relate to the XA models — the XA clusters consist of several 2-8 processor hypernodes while the CD models were shipped with up to 16 processors. Either the CDs are different machines than the XA hypernodes or they are simply two XA hypernodes coupled together, without any additional SCI/CTI expansion possibilities.

Chipset

The chipset is based completely on an own Convex design and centers around the Convex five-port crossbar, later improved on the SPP2000 with eight ports and used in HP's V-Class.

1. **5x5 nonblocking crossbar**, with five crossbar ports, is the central part of the system, it connects to four "functional units" (memory, SCI links and processor) and with the fifth port to the local system I/O. The four functional units contain each a memory controller, SCI controller and an "agent" for two processors. Memory and processor use different data links to the crossbar — memory access *always* goes over the crossbar, even from a processor to the memory in the same functional unit. Each crossbar port has a data rate of 250 MB/s, giving the crossbar a combined peak bandwidth of 1.25 GB/s. The crossbar is implemented in Gallium arsenide gate arrays, GaAs with 250K transistors, a rarity, very expensive and difficult to handle.
2. **Four CPU Agents** attach to the crossbar and provide access for the processors to the memory via the crossbar over a 250 MB/s crossbar port shared with the memory controller.
3. **Four Convex Coherent Memory Controllers CCMCs** attach each one four-way interleaved memory board to the crossbar. The CCMCs additionally do cache coherency and interface to the Convex's SCI (CTI) link for inter-hypernode connection. The CTI interface or the complete CCMC were apparently also GaA chips.
4. **Exemplar I/O subsystem** connects to the fifth 250 MB/s crossbar port and attaches the I/O subsystem controllers to the crossbar and this memory and processors.

Buses

- ◈ Total crossbar bandwidth 1.25 GB/s, five 250 MB/s ports
- ◈ CPU/Memory bandwidth 1.0 GB/s, four 250 MB/s ports shared with memory
- ◈ I/O bandwidth 250 MB/s with one crossbar port
- ◈ *SPP1000* Four SBus I/O buses for expansion slots
- ◈ *SPP1200/SPP1600* Eight SBus I/O buses for expansion slots
- ◈ Attachments to SCI rings, interconnection via four one-dimensional rings bandwidth of 2.4 GB/s
- ◈ SCSI-2 storage I/O bus

Memory

- ◈ DRAM
- ◈ Two to eight memory boards per node
- ◈ Memory is up to eight-way interleaved per node

- *XA single nodes* up to 2 GB of memory (512 MB per memory board)
- *CD nodes* up to 4 GB of memory

Expansion

- *XA single nodes* 8 SBus slots
- *CD nodes* 16 SBus slots
- This is apparently really the same SBus used by Sun in their SPARC workstations

Drives

- 20 internal SCSI drives

3.47.3 Clustering

Multiple SPP1x00/XA systems can be connected together to form a single large system.

- Up two sixteen SPP1000/SPP1200/SPP1600 XA models can be clustered together to form a system with up to
  - 128 processors
  - 32 GB of RAM
  - 64 SBus slots
  - 320 SCSI drives
- Clustered SPP Exemplar are ccNUMA computers.
- Multiple systems (nodes) are connected via four CTI rings: each uni-directional ring attaches to the same CCMC memory controller on different nodes.
- The four rings are implementations of the IEEE Standard 1596-1992 SCI, called by Convex CTI — Convex Toroidal Interconnect.
- Each ring is only unidirectional and has a bandwidth of 600 MB/s, 16-bit differential, 300 MHz clock
- Complete CTI bandwidth is thus 2.4 GB/s.
- Each node's main memory is globally accessible from other nodes on the CTI network: local memory is globally shared.
- Memory access to global memory goes from the processor through the local crossbar to the local functional unit whose memory controller is associated with the remote memory

3.47.4 External

- SCSI depending on installed controller
- Console/control connections for the control workstation, the teststation

Other

- Exemplar 1200 Architecture presentation (FTP, Postscript) Beth Richardson? (N.d.: NCSA. Google archive accessed August 2008)

3.47.5 Operating systems

- Convex SPP-UX, a heavily modified Mach-based operating system, which *looks* familiar to HP-UX but is a completely different design. The later HP V-Class are able to run stock HP-UX, which was modified specially for the V-Class architecture.

3.47.6 Benchmarks

Model	SPEC92 fp	SPEC95 int	SPEC95 fp	SPEC95 *rate*, int	SPEC95 *rate*, fp
SPP1000		3.27	3.98		
SPP1200	185				
SPP1600				8-CPU: 290 16-CPU: 541 32-CPU: 996	8-CPU: 383 16-CPU: 744 32-CPU: 1444

3.47.7 Dimensions

Model	Height	Width	Depth	Weight
SPP1200/XA	71cm	112cm	178cm	404kg
SPP1200/CD	46cm	99cm	89cm	159kg

3.47.8 References

Manuals

- *SPP1200/CD Scalable Computing System*, Convex Data Sheet (1995: Convex Computer Corporation) (URL gone)
- *SPP1200/XA Scalable Computing System*, Convex Data Sheet (1995: Convex Computer Corporation) (URL gone)

Articles

- A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar (Postscript) Robert Castaneda, et al. (1997: in Proceedings of IEEE International Conference on Computer Design (ICCD'97) [there is a mirrored PDF version from citeseer (accessed August 2008)]
- Characterizing Shared Memory and Communication Performance: A Case Study of the Convex SPP-1000 (Postscript) Gheith A. Abandah and Edward S. Davidson (January 1996: University of Michigan. Accessed August 2008)

◈ An Empirical Evaluation of the Convex SPP-1000 Hierarchical Shared Memory System (PDF) Thomas Sterling, et al. (1995: Proceedings of the IFIP WG10.3 working conference on Parallel architectures and compilation techniques. Citeseer mirror accessed April 2009)

3.48 HP/Convex SPP2000 (S-Class/X-Class)

3.48.1 Overview

The HP 9000 S-Class/Convex Exemplar SPP2000 are large scalable PA-RISC computing servers and the direct predecessors of the later HP V-Class (V2200, V2500 et al). Originally developed by Convex, the SPP2000 and later S-Class are based on a crossbar architecture with the central internal "switching" component connecting the resources to each other by forming matrix connections between the devices' input and output ports.

A single SPP2000 computer can hold up to sixteen 64-bit PA-8000 processors with 16 GB of memory in a single *Node* — called *S-Class*. The SPP2000 can form a large-scale system by connecting single Nodes with SCI links into a larger cluster of up to 32 nodes/512 processors. The resulting interconnected system are called *X-Class*, and are are *ccNUMA* computers. The clustering capabilities of their successors, the V2500, have been reduced significantly — in contrast to the 32-node maximum of SPP2000 clusters, V2500s only can be clustered to groups of four.

As the other Exemplar systems, the SPP2000/S-Class are operated and controlled via so-called "teststations," Unix workstations that connect to a central management board in the single nodes which provides booting, system monitoring and diagnostics, and console connections. These teststations were either IBM RS/6000 AIX systems or later, more common, HP 9000 workstation running HP-UX.

3.48.2 System

CPU

- SPP2000 Node/S-Class: 4-16 PA-8000 180 MHz with 1/1 MB off-chip I/D L1 cache each
- SPP2000 Cluster/Wall/X-Class: 32-512 PA-8000 180 MHz with 1/1 MB off-chip I/D L1 cache each

Chipset

The SPP2000 is based on the Exemplar crossbar architecture which connects the CPU and I/O to the system main memory.

1. **8x8 nonblocking crossbar** is the central part of the system, it connects the memory to the processor buses and I/O channels. There are eight ports for "agents" for CPUs and I/O — each agent connects to two CPUs and one I/O channel — , and eight ports for memory. Each crossbar port has a path width of 64-bit, giving it 960 MB/s peak bandwidth. The peak bandwidth of the crossbar is 15.3 GB/s combined. The crossbar in the original SPP1x00 Exemplar design was built with GaA chips, the SPP2000 in standard CMOS with 1.1M transistors.
2. **Eight Data Mover/Agents** attach to the crossbar and provide access for the processors with Runway buses and I/O controllers to the memory via the crossbar over a 1.9 GB/s datapath with four 32-bit, unidirectional buses from two ports on the Agent connect to two crossbar ports. The I/O channels on the agent have a maximum bandwidth of 240 MB/s. Each Agent has two Runway processors buses with an aggregate bandwidth of 960 MB/s.
3. **Eight PCI controller** connect the 240 MB/s I/O channels/PCI buses to the Agents.

4. **Eight Memory controllers** attach each one four-way interleaved memory board to the Hyperplane crossbar. Each Memory controller has a bandwidth of 1.9 GB/s. The memory controllers probably also interface with the CTI interconnection.

Buses

- Total crossbar bandwidth 15.3 GB/s (intra-crossbar)
- CPU bandwidth 7.5 GB/s (CPU-to-Agent, eight Runway 960 MB/s buses)
- Memory bandwidth 15 GB/s (memory-to-crossbar, sixteen 960 MB/s links)
- I/O bandwidth 1.9 GB/s (eight 240 MB/s channels, I/O channel-to-Agent)
- Eight PCI-32 I/O buses for expansion slots (each 240 MB/s)
- Attachments to SCI rings/CTI ("Coherent Toroidal Interconnect") via two rings (X-ring and Y-ring), Node-to-Node bandwidth of 3.84 GB/s, the rings operate at a clock of 120 MHz with a width of 32 bit
- SCSI-2 Ultra main storage I/O bus

Memory

- SDRAM DIMMs
- Two to eight memory boards per node
- Memory is up to four-way interleaved per memory board and up to 32-way interleaved per node
- SPP2000 Node/S-Class: 1 GB minimum, 16 GB maximum
- SPP2000 Wall/X-Class: 512 GB maximum (with 32 nodes)

Expansion

- 24 PCI 32-bit slots on eight PCI 32-bit channels

Drives

- 20 internal Ultra SCSI drives

3.48.3 Clustering

Multiple Exemplar SPP2000/HP S-Class systems can be connected together to form a single large system, a "Wall" /X-Class.

- Up two 32 single nodes can be clustered together to form a system with up to
  - 512 processors
  - 512 GB of RAM

- 768 PCI slots
- 640 SCSI drives

◈ Clustered SPP2000s/X-Class are ccNUMA computers; they are not fully conformant to the PA-RISC 2.0 specification (and thus do not run standard HP-UX).

◈ Multiple systems are connected via two CTI rings: these links attach to the eight memory controllers of a node. A single system attaches to other single "nodes" and their respective crossbars with a node-to-note data rate of 3.8 GB/s.

◈ The two rings are called X-ring and Y-ring.

◈ The links are implementations of the IEEE *SCI* from Convex — Convex Toroidal Interconnect.

◈ Each node's main memory is globally accessible from other nodes on the CTI network (that is, local memory is globally shared).

◈ A part of each system's main memory is reserved for cache memory for the CTI network (configured statically at boot time).

3.48.4 External

◈ 68-pin VHDCI Ultra LVD external SCSI

◈ Three Serial RS232C DB9 (local console, remote console, general purpose) via a DB25 "M cable"

◈ 10/100 Mbit Ethernet TP/RJ45

◈ 10/100 Mbit Ethernet TP/RJ45 *LAN console*

3.48.5 Operating systems

◈ Convex SPP-UX, a heavily modified Mach-based operating system, which *looks* familiar to HP-UX but is a completely different design. The later HP V-Class are able to run stock HP-UX (which was modified specially for the V-Class architecture).

3.48.6 Benchmarks

Model	**SPEC95 int**	**SPEC95 fp**	**SPEC95 *rate*, int**	**SPEC95 *rate*, fp**
SPP2000/S-Class/X-Class	11.8	18.7	92.5 2-CPU: 183 4-CPU: 363 6-CPU: 539 8-CPU: 713 10-CPU: 867 12-CPU: 1012 16-CPU: 1307	141 2-CPU: 276 4-CPU: 524 6-CPU: 739 8-CPU: 935 10-CPU: 1085 12-CPU: 1220 16-CPU: 1413

3.48.7 Dimensions

Height	Width	Depth	Weight
736mm	914mm	889mm	250kg

3.48.8 References

Articles

- Exemplar System Architecture Hewlett-Packard/Convex (Januar 1997, archive.org mirror, access August 2008)
- SPP 2000 Architecture presentation (FTP, Postscript) Beth Richardson (N.d.: NCSA. Google archive accessed August 2008)
- A Comparative Evaluation of Hierarchical Network Architecture of the HP-Convex Exemplar (Postscript) Robert Castaneda, et al. (1997: in Proceedings of IEEE International Conference on Computer Design (ICCD'97) [there is a mirrored PDF version from citeseer (accessed August 2008)]

3.49 HP 9000/T500, T520, T600 and 890

3.49.1 Overview

The HP 9000 T-Class servers were large 32-bit PA-RISC mainframes from the mid-1990s, built with modular system cards that contain processors, memory or I/O devices. The main system backplane features sixteen slots, eight of which can be used for memory or processor boards, and the other eight for I/O boards and converters. These boards plug into the main system VSC bus at 60 MHz.

The HP 9000/890 was an early iteration of the architecture, with the later T500/T600 being updated sucessors. After the 64-bit T600 T-Class design was discontinued in favor of the more flexible Superdome systems.

Apparently 890 and T500 could be board-upgraded to T520, with an board-upgrade path to PA-8000 processors as well.

System	Model number	Introduced	Price
890	HP 9000/890	1992	
T500	HP 9000/891	1993/1994	$165,000 uni$660,000 12-way
T520	HP 9000/892	1995	$145,000 uni$520,000 14-way
T600	HP 9000/893	1997	

3.49.2 System

CPU

- 890: 1-4 PA-7000[1] 60 MHz with 4 MB off-chip L1 cache
- T500: 1-12 PA-7100 90 MHz with 2 MB off-chip L1 cache
- T520: 1-14 PA-7150 120 MHz with 2 MB off-chip L1 cache
- T600: 1-12 PA-8000 180 MHz with 2 MB off-chip L1 cache and 8 MB off-chip L2 cache[3]

Notes

1. Not sure if this is really a PA-7000, the documentation is not very explicit
2. The off-chip caches of the CPUs are rather large — especially on the 890 server
3. The T600 was apparently the only system with a PA-8000 processor with L2 cache, while an L2 cache was not even mentioned on the PA-8000 documentation

Processor cards

The processor cards attach the processors and support chips to the main system bus via slots for processors, memory and I/O cards.

The 890 and the T-Class have slighly different architectures:

9000/890

- Processor cards contain eight VLSI CMOS chips:

1. PA-7000 CPU main processor
2. Cache chips ICMUX, DCMUX0 and DCMUX1 for 2 MB I and 2 MB D cache, ECC
3. Floating point processor FPC, MUL and ADD
4. Viper system bus VSC interface

◈ Up to four processor cards per system

The chip configuration looks like a PCX processor, with CMUX and FP chips, the other parameters contradict this however, including the (main memory, clock speed, bus interfaces.

T500, T520 and T600

◈ Processor cards contain each up to two processor modules with the actual CPUs

◈ Up to six cards in T500/T600 or seven in T520 per system

◈ Processor card chips:

1. Two Viper system bus VSC interface
2. Bus support chips
3. *T600* 4 MB L2 I cache and 4 MB L2 D cache, each two modules

◈ Processor module chips:

1. *T520/T500*PA-7100 CPU main processor
2. *T600*PA-8000 CPU main processor
3. 1 MB L1 I cache
4. 1 MB L1 D cache

Chipset

The chipsets depend on the plug-in I/O cards.

◈ Viper processor to system bus interface, integrated on processor cards

◈ HP-PB to VSC bus converter, integrated on the HP-PB interface cards

◈ Common HP-PB plug-in cards:

- Fast/Wide SCSI
- MUX
- LAN/console
- HP-FL fiber link interface

◈ *T600* HP-HSC I/O Bus Converter

◈ Service processor, controls all hardware and power of the system, integrated into a single-board located in the main cardcage

Buses

- PBus processor/memory bus, 60 MHz, 32-bit data path between single CPUs and their Viper main bus interfaces, that means one PBus per processor card on 890 servers, two PBuses per card on all others, 240 MB/s each
- VSC central system bus, 60 MHz clock
  - 890: 32-bit wide with 240 MB/s data rate
  - T500/T520: 64-bit wide with 480 MB/s data rate
  - T600: 128-bit wide with 960 MB/s data rate
- PBus and VSC are configured for PBus Variant 2 "Scalable MP" multiprocessing attachment
- *T600*Runway CPU/memory bus, although not mentioned in documentation
- *T600*GSC+ expansion bus in HSC variant
- HP-PB bus for general I/O,
- SCSI depends on installed I/O cards

Memory

- Memory cards, in sizes of 64-768 MB, not all systems support all cards
- Up to eight cards in P MB card slots 1-14
- Memory attaches to shared VSC system bus, 64-bit data path, and 128-bit data path on T600
- Cards operate at VSC bus frequency and have on-card interfaces to VSC bus
- *890* max 2 GB main memory
- *T500/T520/T600* max 3.75 GB main memory

Expansion

- *T600* 24 HSC/GSC+ slots, depends on HP-PB slot usage
- 14 HP-PB slots single-height — 7 double-height
- Up to 98 additional HP-PB slots can be added through "expanion cabinets"

Drives

- Drives located in external drive bays or racks

3.49.3 External

- SCSI-2 50-pin single-ended
- TP/RJ45 10BaseT 10 Mbit Ethernet

- Two Serial RS232C DB9, one for console, one for USV
- Parallel DB25
- Two PS/2 connectors for keyboard und mouse

3.49.4 Operating systems

- 890 servers: HP-UX up to 10.20 for 800s servers.
- T-Class: HP-UX 10.20 for 800s servers, 11.00 and 11i v1

3.49.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp	SPEC95 *rate*, int	SPEC95 *rate*, fp
T520			5.2		1-CPU: 47.2 2-CPU: 93.8 4-CPU: 186 8-CPU: 363 12-CPU: 531	
T600			11.8	14.9	1-CPU: 106 2-CPU: 211 4-CPU: 418 6-CPU: 617 8-CPU: 814 10-CPU: 1003 12-CPU: 1192	1-CPU: 134 2-CPU: 263 4-CPU: 510 6-CPU: 735 8-CPU: 915 10-CPU: 1043 12-CPU: 1151

3.49.6 Dimensions

Height	Width	Depth	Weight
1620mm	750mm	905mm	360kg

3.49.7 References

Manuals

- CE Handbook HP 3000 99x Family, HP T-Class Family (URL gone)
- Installation Guide T-Class HP 3000 99x Family, HP 9000 Systems (URL gone)
- Operator's Guide HP 3000 99x Family, HP 9000 T-Class Systems (URL gone)

Articles

- Corporate Business Servers: An Alternative to Mainframes for Business Computing (.pdf) Thomas B. Alexander et al (June 1994: Hewlett-Packard Journal)

◈ HEWLETT-PACKARD MOVES T-CLASS SERVERS UP TO PA-7150 RISCS, Computer Business Review September 1995

3.50 HP V2200 and V2250

3.50.1 Overview

The HP 9000 V2250 and V2250 are large-scale scalable PA-RISC servers, with up to sixteen 64-bit PA-RISC processors in a single cabinet. They are based on a crossbar architecture — one central internal "switching" component links the various computing resources to each other by connecting the devices' inputs to other devices' output ports, in effect forming matrix connections. The V2200 and V2250 use HP's own HyperPlane crossbar chipset, consisting of four central crossbar ASICs and various other chipset components to attach memory, processors and I/O.

The architecture is a direct continuation from the Convex *Exemplar* — the earlier Convex/HP 32-bit SPP1x00 and 64-bit SPP2000 S-Class/X-Class, use a similar crossbar-based system design. The V2200/V2250 use a very similar design to the SPP2000 S-Class, minus the SCI/TCI links for interconnecting several nodes into a larger syste The V2500/V2600 successors were delivered again with the interconnection technology.

The V2200s and V2250s are controlled via a so-called "teststation," which runs its own HP-UX operating system and controls and monitors the V-Class server. This teststation is a standard HP 9000/712 workstation with special teststation hardware, such as a second ethernet and serial boards, and software. The teststation connects to the Core Utilities Board CUB, which provides booting, system monitoring and diagnostics, and console connections via one LAN and one special serial link.

3.50.2 System

CPU

- V2200: 4-16 PA-8200 200 MHz with 4 MB off-chip L1 cache each
- V2250: 4-16 PA-8200 240 MHz with 4 MB off-chip L1 cache each

Chipset

The V-Classes are based on the HP HyperPlane crossbar which connects the CPU and I/O to the system main memory.

1. HyperPlane crossbar, 8x8, non-blocking, consists of four Exemplar Routing Attachment controllers ERACs and is the central part of the system, it connects the memory to the processor buses and I/O channels. There are eight ports for "agents" for CPUs and I/O — each agent connects to two or four CPUs and one I/O channel — , and eight ports for memory. Each crossbar port has a data path of 64-bit, giving it 960 MB/s peak bandwidth. The peak bandwidth of the HyperPlane crossbar/ERACs is 15.3 GB/s combined.
2. Eight Exemplar Processor Agent controllers EPACs attach to the crossbar and provide access for each two processors Runway buses and one I/O controller to the memory via the crossbar over a 1.9 GB/s datapath, four 32-bit, unidirectional buses from two ports on the PAC connect to two Hyperplane crossbar ERACs; each EPAC thus communicates with only two of the system's four ERACs. The I/O channels on the agents have a maximum bandwidth of either 120 or 240 MB/s. Each EPAC has two Runway processors buses, 64-bit, bidirectional, which have an aggregate peak bandwidth of 960 MB/s for two processors per EPAC.

3. Eight Exemplar PCI-bus Interface controller EPICs connect the 240 MB/s I/O channels/PCI buses to the EPACs.
4. Eight Exemplar Memory Access controllers EMACs attach each one 32-way interleaved memory board to the Hyperplane crossbar. Each EMAC has a bandwidth of 1.9 GB/s, four 32-bit, unidirectional buses from two ports on the EMAC connect to two Hyperplane crossbar ERACs.
5. The Exemplar Core Utilities board ECUB provides interrupts and the central system logic, it connects to the Exemplar system Routing board ENRB. The Core Logic Bus from the ECUB attaches to the devices on the EPACs. Included on the ECUB are two custom FPGAs, the Exemplar Processor Utilities controller EPUC and the Exemplar Monitoring Utilities controller EMUC.

The remainder of the system I/O consist of standard HP PCI controllers, frequently:

- PCI Fast-wide FWD SCSI controller, high-voltage differential/HVD)
- PCI fibrechannel FC controller

Buses

- Total crossbar bandwidth 15.3 GB/s, intra-crossbar
- CPU bandwidth 7.5 GB/s, CPU-to-EPAC, eight Runway 960 MB/s buses
- Memory bandwidth 15 GB/s, memory-to-crossbar, sixteen 960 MB/s links
- I/O bandwidth 1.9 GB/s, eight 240 MB/s channels, I/O channel-to-EPAC
- Eight PCI-64/33 I/O buses for expansion slots, each 240 MB/s
- SCSI/storage buses depend on the installed SCSI adapter

Memory

- SDRAM DIMMs
- Two to eight memory boards, each memory board has 16 slots
- Memory is up to 32-way interleaved
- 16 GB maximum

Expansion

- 24 PCI 64-bit 33 MHz slots on eight PCI 64-bit channels

Drives

- 16 internal SCSI drives, exact type depending on installed SCSI adapter

3.50.3 External

- External SCSI connection
- Serial and two Ethernet for the console/Teststation

3.50.4 Operating systems

- HP-UX: 11.00 and 11i v1 (v1)

3.50.5 Benchmarks

Model	**SPEC95 int**	**SPEC95 fp**	**SPEC95 *rate*, int**	**SPEC95 *rate*, fp**
V2200	13.8	22.1	1-CPU: 125 4-CPU: 484 8-CPU: 964 12-CPU: 1442 16-CPU: 1865	1-CPU: 4-CPU: 755 8-CPU: 1380 12-CPU: 1909 16-CPU: 2312
V2250	16.4	24.8	16-CPU: 2209	16-CPU: 2471

3.50.6 Dimensions

Height	**Width**	**Depth**	**Weight**
1006mm	998mm	859mm	250kg

3.50.7 References

- Site Preparation Guide: HP 9000 V-Class Server Hewlett-Packard Development Company (March 1998, second edition, A3725-96021)
- Upgrade Guide HP V2200 to V2250 (PDF) Hewlett-Packard Company (March 1998, edition 1, A5083-90001)
- Architecture HP 9000 V-Class Server (PDF) Hewlett-Packard Company (March 1998, second edition, A3725-96022)

3.51 HP V2500 and V2600

3.51.1 Overview

The HP 9000 V2500 and V2600 are second generation scalable PA-RISC V-Class servers based on the Convex Exemplar architecture with up to 32 64-bit PA-RISC processors in a single cabinet. As their Convex SPP2000 predecessors, and contrary to their V2200/V2250 cousins, up to four systems can be interconnected via CTI links. The resulting combined system can have up to 128 CPUs and appears to the operating system as a single computer. Architecturally the interconnected V2500s/V2500s are ccNUMA computers.

The V-Class servers are based on a crossbar architecture — one central internal "switching" component links the various computing resources to each other by forming matrix connections. The V2500 and V2600 use HP's own HyperPlane crossbar chipset, consisting of four central crossbar ASICs and various other chipset components to attach memory, processors and I/O.

The architecture is a direct continuation from the Convex *Exemplar* — the HP/Convex SPP1x00 and SPP2000 S-Class and X-Class use a similar crossbar system design based on GaA chips which was upgraded for the V-Class with faster processors and memory. A multi-node V2500/V2600 system architecture, SCA, does not conform fully to the PA-RISC 2.0 reference architecture — the firmware layer emulates a reference-compliant PA-RISC system for the operating system. However several changes had to be made to the HP-UX kernel to accomodate the V-Class's special architecture, also called "technical anomalies."

The V2500s and V2600s are controlled via a "teststation" , also called SSP, Service Support Processor, that runs its own operating system and controls and monitors the V-Class server, a a HP 9000/712 or B180L workstation. Earlier Convex systems apparently used IBM RS/6000 workstations running AIX to control the Exemplar systems. The SSP/teststation connects to the Core Utilities Board CUB, which provides booting, system monitoring and diagnostics, and console connections, connected via one LAN and one special serial link.

3.51.2 System

CPU

- V2500: 2-32 PA-8500 440 MHz with 512/1024 KB on-chip I/D L1 cache each
- V2600: 2-32 PA-8600 552 MHz with 512/1024 KB on-chip I/D L1 cache each

Chipset

The V-Class V2500 and V2600 are based on the HP HyperPlane crossbar which connects the CPU and I/O to the system main memory.

1. HyperPlane crossbar, 8x8, non-blocking, consists of four Routing Attachment controllers RACs and is the central part of the system, it connects the memory to the processor buses and I/O channels. There are eight ports for "agents" for CPUs and I/O — each agent connects to two or four CPUs and one I/O channel — , and eight ports for memory. Each crossbar port has a path width of 64-bit, giving it 960 MB/s peak bandwidth. The peak bandwidth of the HyperPlane crossbar/RACs is 15.3 GB/s combined.

2. Eight Processor Agent controllers (PACs), also SPAC, attach to the crossbar and provide access for the processor Runway buses and I/O controllers to the memory via the crossbar over a 1.9 GB/s datapath, four 32-bit, unidirectional buses from two ports on the PAC connect to two Hyperplane crossbar RACs; each PAC thus communicates with only two of the system's four RACs. The I/O channels on the agent have a maximum bandwidth of 240 MB/s. Each PAC has two Runway processors buses with an aggregate peak bandwidth of 960 MB/s.
3. Eight PCI-bus Interface controller (SAGA) connect the 240 MB/s I/O channels/PCI buses to the PACs.
4. Eight Memory Access controllers (MACs), also SMAC, attach each one 32-way interleaved memory board to the Hyperplane crossbar. Each MAC has a bandwidth of 1.9 GB/s, four 32-bit, unidirectional buses from two ports on the MAC connect to two Hyperplane crossbar RACs
5. The Core Utilities board (CUB) provides interrupts and the central system logic, it connects to the Midplane Interconnect Board MIB. The Core Logic Bus from the CUB attaches to the devices on the PACs.
6. Eight Toroidal Access Controller (STACs) connect to a variation of the Scalable Coherent Interconnect SCI to one or two "rings." The combination of STACs and SCI rings is referred to as Coherent Toroidal Interconnect CTI.

The remainder of the system I/O consist of standard HP PCI controllers, frequently shipped in default configuration with one of the following:

- ◈ PCI Fast-wide SCSI controller high-voltage differential/HVD
- ◈ PCI Ultra2-wide SCSI controller low-voltage differential/LVD
- ◈ PCI fibrechannel (FC) controller

Buses

- ◈ Total crossbar bandwidth 15.3 GB/s, intra-crossbar
- ◈ CPU bandwidth 7.5 GB/s, CPU-to-PAC, eight Runway 960 MB/s buses
- ◈ Memory bandwidth 15 GB/s, memory-to-crossbar, sixteen 960 MB/s links
- ◈ I/O bandwidth 1.9 GB/s, eight 240 MB/s channels, I/O channel-to-PAC
- ◈ PAC bandwidth, PAC-to-crossbar is also 15 GB/s theoretically, with sixteen 960 MB/s links for the eight PACs
- ◈ Eight PCI-64/33 I/O buses for expansion slots, each 240 MB/s
- ◈ Attachments to CTI/Scalable Computing Architecture SCA crossbar interconnection, 3.8 GB/s
- ◈ SCSI/storage buses depend on the installed SCSI adapter, most likely either Fast-wide or Ultra2-wide

Memory

- ◈ SDRAM DIMMs, 88-bit or 80-bit
- ◈ Two to eight memory boards

- Each memory board has 16 slots: four 4-slot "quadrants"
- Memory is up to 256-way interleaved
- 1 GB minimum
- 32 GB maximum

Expansion

- 28 PCI 64-bit 33 MHz slots on eight PCI 64-bit channels

Drives

- 16 internal SCSI drives, exact type depending on installed SCSI adapter

3.51.3 Clustering

Multiple V-Classes can be connected together to form a single large system resulting in a "SCA", a scalable Computing Architecture system. Up two four V2500/V2600s can be clustered together to form a system with up to 128 processors, 128 GB of RAM, 112 PCI slots and 64 SCSI drives. Clustered V-Classes are ccNUMA computers and do not conform fully to the PA-RISC 2.0 specification.

Multiple systems are connected via two CTI rings: these links attach via the STACs to the eight memory controllers. The two rings are called X-ring and Y-ring. Each system attaches to one or two other V2500/V2600 cabinets and their respective crossbars with a node-to-note data rate of 3.8 GB/s. The links are implementation of the IEEE SCI standard taken over from Convex — Coherent Toroidal Interconnect or Convex Toroidal Interconnect. Each node's main memory is globally accessible from other nodes on the CTI network, that is, local memory is globally shared. 32-512 MB of each system's main memory is reserved for cache memory for the CTI network configured statically at boot time.

3.51.4 External

- SCSI depends on installed adapter, either Ultra or Fast wide
- Serial and Ethernet connections of the teststation/SSP

3.51.5 Operating systems

- HP-UX: 11.00 and 11i v1 (v1)

3.51.6 Benchmarks

Model	**SPEC95 *rate*, int**
V2500	16-CPU: 400232-CPU: 7481
V2600	16-CPU: 516432-CPU: 9315

3.51.7 Dimensions

Height	Width	Depth	Weight
990mm	800mm	940mm	223kg

3.51.8 References

Manuals

- Operator's Guide HP 9000 V2500 Server (PDF) Hewlett-Packard Company (December 1998, first edition, A5075-90005)
- Installation Guide HP 9000 V2500 Server (PDF) Hewlett-Packard Company (December 1998, first edition, A5075-90001)
- Diagnostics Guide HP V2500/V2600 Servers (PDF) Hewlett-Packard Company (December 1999, first edition, A5824-96002)
- Upgrade Guide HP V2500/V2600 Servers (PDF) Hewlett-Packard Company (December 1999, first edition, A5824-96004)

Articles

- Architecture Reference Guide V2500 Server (PDF) Hewlett-Packard Company (June 1999, first edition, A5074-90004)
- HP Scalable Computing Architecture Randy Wright and Arun Kumar (October 2000/revised January 2002: USENIX, Proceedings of the First WIESS Workshop)

3.52 HP zx2000

3.52.1 Overview

The HP zx2000 Itanium workstations are closely based on the PA-RISC C8000 workstations build around the same HP *zx1* chipset. The system is built in a sleek and quiet tower casing and also available with a rack-mount option. Relative shortly after the zx2000 HP dropped Itanium *workstations* from its portfolio. The remaining HP-UX/Itanium offerings are IA64 server systems (the *Integrity rx*).

3.52.2 System

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1	Itanium 2 *McKinley*	900 MHz	16/16 KB	256 KB	1.5 MB
1	Itanium 2 *Madison*	1.4 GHz	16/16 KB	256 KB	1.5 MB
1	Itanium 2 *Madison*	1.4 GHz	16/16 KB	256 KB	4.0 MB
1	Itanium 2 *Madison*	1.5 GHz	16/16 KB	256 KB	1.5 MB
1	Itanium 2 *Deerfield*low-voltage	1.0 GHz	16/16 KB	256 KB	1.5 MB

There could be more processor options.
All caches are on-die (L1, L2 and L3).

Chipset

- HP zx1 chipset (same as in some PA-8800/PA-8900 workstations)
  - Pluto zx1 MIO (memory and I/O controller) connects to the processor bus (6.4 GB/s), memory bus (4.25 GB/s) and six I/O channels (aggregate 3.0 GB/s) and contains both memory and cache controllers
  - Four zx1 IOAs (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 3.0 GB/s on six 0.5 GB/s channels
    1. AGP 4x graphics bus on two channels — 1.0 GB/s
    2. PCI-X 64/133 I/O slot on two channels — 1.0 GB/s
    3. Four PCI-X 64/66 I/O slots on one channel — 0.5 GB/s
    4. Gigabit Ethernet, IDE, USB and audio controllers on PCI 32/33 on one channel — 0.5 GB/s
- Gigabit Ethernet (Intel 82540)
- Two-channel Ultra160 SCSI controller (optional)
- Ultra ATA-100 IDE controller (PCI649)
- PDH controller
- Serial controller, DUART (16550A-compatible)
- FPGA controller for ACPI (2.0) and LPC

- Baseboard management controller (BMC — IPMI interface)

Buses

- Itanium 2/zx1 processor bus 6.4 GB/s
- zx1 memory bus, 200 MHz, 4.25 GB/s
- Six zx1 I/O channels/buses, aggregate 3.0 GB/s I/O bandwidth
- AGP 4x graphics bus on two I/O channels, 1.0 GB/s aggregate
- PCI-X 64/133 I/O bus on two I/O channels, 1.0 GB/s aggregate
- PCI-X 64/66 I/O bus on one I/O channel, 0.5 GB/s aggregate
- PCI 32/33 I/O bus for onboard devices on one I/O channel, 0.5 GB/s aggregate
- SCSI-3 Ultra160 (LVD) storage I/O bus (if optional SCSI controller is installed)
- UltraATA-100 IDE storage I/O bus

Memory

- PC2100 registered ECC DDR266 SDRAM DIMMs
- Takes up to 2 GB modules
- Four slots
- 512 MB minimum (2×256 MB)
- 8 GB maximum (4×2 GB)
- 4.25 GB/s memory bandwidth

Expansion

- One PCI-X 64-bit/133 MHz slot, full-length
- Three PCI-X 64-bit/66 MHz slots, full-length
- One PCI-X 64-bit/66 MHz slot, half-length
- All PCI slots are 3.3 V
- One AGP Pro 4x 32-bit slot, 1.5 V

Drives

- Up to two internal 3.5âĂş bays for either Ultra ATA-100 IDE or Ultra160 SCSI hard drives
- Two half-heigth 5.25âĂş bays for externally accessible Ultra ATA-100 IDE or SCSI (LVD or SE) drives (DVD/CD)

3.52.3 External

- TP/RJ45 Gigabit Ethernet
- Four USB 2.0 ports (two in front, two in rear)
- Two Serial RS232C DB9
- Four phone jacks (microphone, line-in and line-out) on 16-bit audio card
- Optional IEEE-1394 Firewire ports

3.52.4 Operating systems

- HP-UX11i v1.6 and 11i v2
- Linux for Itanium
- FreeBSD/ia64
- OpenVMS (however officially unsupported on this platform)
- Windows XP 64-Bit Edition Version 2003
- Windows Server 2008 Itanium-based Editions
- Windows Server 2003 Itanium-based Editions

3.52.5 Benchmarks

Model	**SPEC2000, int**	**SPEC2000, fp**	**SPEC2000*rate*, int**	**SPEC2000*rate*, fp**
zx2000900 MHz	668	1086		12.6

3.52.6 Dimensions

Model	**Height**	**Width**	**Depth**	**Weight**
Tower	502mm	268mm	512mm	25kg
Rack-mounted	4U	482mm	510mm	20kg

3.52.7 References

Manuals

- HP Workstation zx2000 - Technical Reference Guide (URL gone)

3.53 HP zx6000

3.53.1 Overview

The HP zx6000 are dual-processor Itanium workstations based on the zx2000 workstation with an architecture centered around the HP zx1 Itanium chipset, also used in the zx2000 and PA-RISC servers. The chassis was designed for rack-mounting (2U) with appropriate rails; with a tower kit it can be converted to a standalone unit. In contrast to the zx2000, the zx6000 has slightly higher I/O and double the memory bandwidth and supports three times the amount of memory.

The zx6000 with fast CPUs is probably the fastest HP-UX workstation.

3.53.2 System

CPU

No.	CPU Type	Clock	L1 (I/D)	L2 (I/D)	L3
1-2	Itanium 2 *McKinley*	900 MHz	16/16 KB	256 KB	1.5 MB
1-2	Itanium 2 *McKinley*	1.0 GHz	16/16 KB	256 KB	3.0 MB
1-2	Itanium 2 *Madison*	1.3 GHz	16/16 KB	256 KB	3.0 MB
1-2	Itanium 2 *Madison*	1.5 GHz	16/16 KB	256 KB	6.0 MB

All caches are on-die (L1, L2 and L3).

Chipset

- HP **zx1** chipset
  - Pluto zx1 MIO (memory and I/O controller) connects to the processor bus (6.4 GB/s), two memory buses (each 4.25 GB/s) and seven I/O channels (aggregate 3.5 GB/s) and contains both memory and cache controllers
  - Six **zx1 IOAs** (I/O adapters) connect the PCI-X slots and I/O devices to the zx1 MIO with an aggregate bandwidth of 3.5 GB/s on seven 0.5 GB/s channels
    1. AGP 4x graphics bus on two channels — 1.0 GB/s
    2. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
    3. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
    4. PCI-X 64/133 I/O slot on one channel — 0.5 GB/s
    5. Gigabit Ethernet and Ultra320 SCSI on PCI 64/66 on one channel — 0.5 GB/s
    6. IDE, USB, management LAN on PCI 32/33 on one channel — 0.5 GB/s
- Gigabit Ethernet (Broadcom 5701)
- Two-channel Ultra320 SCSI controller (LSI 1030)
- Ultra ATA-100 IDE controller (PCI649)
- PDH controller

- Serial controller, DUART (16550A-compatible)
- FPGA controller for ACPI (2.0) and LPC
- Baseboard management controller (BMC — IPMI interface)
- 10/100 Ethernet for management (Intel 82550)

Buses

- Itanium 2/zx1 processor bus 6.4 GB/s
- Two independent zx1 memory buses, 266 MHz, each 4.25 GB/s — aggregate 8.5 GB/s memory bandwidth
- Seven zx1 I/O channels/buses, aggregate 3.5 GB/s
- Three PCI-X 64/133 I/O buses
- PCI-X 64/66 I/O bus (for SCSI/Gigabit Ethernet onboard)
- PCI 32/33 I/O bus (for IDE/USB/management onboard devices)
- Two SCSI-3 Ultra320 (LVD) storage I/O buses
- AGP 4x graphics bus
- UltraATA-100 IDE storage I/O bus

Memory

- PC2100 registered ECC DDR266 SDRAM DIMMs
- Takes up to 2 GB modules
- Twelve slots
- 512 MB minimum (2×256 MB)
- 24 GB maximum (12×2 GB)
- 8.5 GB/s memory bandwidth

Expansion

- Three PCI-X 64-bit/133 MHz slots, full-length
- All PCI slots are 3.3 V
- One AGP Pro 4x 32-bit slot, 1.5 V

Drives

- Three internal 3.5âĂș bays for Ultra160 SCSI SCA 80-pin hard drives, hot-plug
- Slimline bay for optional IDE CD or DVD drive

Drive 1 and 2 are on one SCSI channel, drive 3 and the external connector are on the second SCSI channel.

3.53.3 External

- Gigabit Ethernet, TP/RJ45
- 10/100 Ethernet, TP/RJ45 BT management network
- Ultra320 SCSI 68-pin
- 25-pin serial for management processor card, needs break-out cable for three serial ports
- Four USB 2.0 ports
- Two Serial RS232C DB9

3.53.4 Operating systems

- HP-UX11i v1.6 and 11i v2
- Linux for Itanium
- FreeBSD/ia64
- Windows Server 2008 Itanium-based Editions
- Windows Server 2003 Itanium-based Editions
- Windows XP 64-Bit Edition Version 2003
- OpenVMS (however officially unsupported on this platform)

3.53.5 Benchmarks

Model	SPEC2000, int	SPEC2000, fp	SPEC2000*rate*, int	SPEC2000*rate*, fp
zx6000900 MHz	669	1139	7.8 2-CPU: 15.4	13.2 2-CPU: 23.9
zx6000 1.0 GHz	807	1422		16.5 2-CPU: 30
zx6000 1.5 GHz	1315	2106	15.2 2-CPU: 30.4	24.4 2-CPU: 42.4

3.53.6 Dimensions

Model	Height	Width	Depth	Weight
Tower	494mm	295mm	675mm	25kg
Rack-mounted	2U	483mm	679mm	22kg

3.53.7 References

Manuals

- Operation and Maintenance Guide HP Integrity rx2600 server and HP workstation zx6000 (PDF) Hewlett-Packard Development Company (September 2003, second edition)

3.54 RDI PrecisionBook

3.54.1 Overview

The RDI Tadpole PrecisionBook portable PA-RISC workstations, introduced in 1998, are HP 9000 C132L/C160L workstations in a portable case. A major addition to the desktop design is the integrated Cardbus controller for which Tadpole supplied a driver kit for HP-UX.

Since the RDI PrecisionBooks were technically more or less C132L/C160Ls, they supported the same standard PA-RISC operating systems and applications. Their laptop case was used for other RDI RISC laptops as well, for example the UltraSPARC.

Table 3.129: RDI PrecisionBook model number, release date and prices

Model	Number	Introduced	Price
PrecisionBook 132 12″	9000/779	1998	$11,995
PrecisionBook 160 14″	9000/779	1998	$14,995
PrecisionBook 180	9000/779	1998	

There were only two other portable PA-RISC computers produced — the SAIC Galaxy 1100, based on HP 9000 712, and the Japanese Hitachi 3050RX/100C.

3.54.2 System

CPU

- PrecisionBook 132: PA-7300LC 132 MHz with 128 KB on-chip L1 (and 1 MB off-chip L2) cache
- PrecisionBook 160: PA-7300LC 160 MHz with 128 KB on-chip L1 (and 1 MB off-chip L2) cache
- PrecisionBook 180: PA-7300LC 180 MHz with 128 KB on-chip L1 (and 1 MB off-chip L2) cache

The external L2 cache was optional but was supplied with most systems.

Chipset

- LASI integrated chipset
- (integrated) NCR 53C710 8-bit single-ended SCSI-2
- (integrated) Intel 82596CA 10 Mbit Ethernet controller
- (integrated) Harmony CD/DAT quality 16-bit stereo audio
- Phantom PseudoBC GSC+ port
- Dino GSC-to-PCI bridge
- Visualize-EG (*Graffiti*) graphics with 2MB frame buffer memory
- 1 MB flash memory
- Two Cirrus CL-PD6832 PCI-CardBus bridges
- CMD PCI0643 IDE/UDMA33 controller

Display

- Integrated display, option of 12.1âĂş (0.24mm dot pitch) or 14.1âĂş (0.28mm dot pitch) active matrix LCD (the 14-inch version were most popular)
- XGA resolution (1024×768), 16M colors, 60Hz refresh
- External monitor output supports VGA, SVGA, XGA, SXGA and 1600×1200 resolutions at refresh rates of 60, 72 and 75Hz
- At XGA resolution the LCD and external monitor can be used at the same time, with different resolutions on the external monitor the LCD blanks

Input

- PS/2-compatible, 97-key keyboard
- Three-button trackpad

Energy

- Lithium-Ion battery with 40Wh capacity, 450g, 0.5-1 hours battery time
- Recharge time of 2.5 hours when powered off
- Laptop draws about 70W continous
- AC adapter provides 19V (DC) 3.68A, non-standard pinout

Buses

- GSC-2 general system-level I/O bus
- PCI-32/33 device I/O bus
- SCSI-2 Fast-Narrow single-ended bus disk I/O
- PDH bus, peripheral interface connecting to flash memory, NVRAM and PSM bus
- PSM bus, provides connection to the power-supply module

Memory

- Two sockets for 32 – 512 MB (2×256)
- Proprietary ECC modules, 32-256 MB modules, 60ns, 144-bit wide

Expansion

- Two Cardbus slots, for Cardbus and PCMCIA expansion cards

Drives

- Two 2.5âĂș IDE hard drives with SCSI converter or 2.5âĂș SCSI drives
- Since 2.5-inch SCSI drives are uncommon RDI used regular IDE notebook drives with a special IDE-SCSI converter from ADTX)

3.54.3 External

- SCSI-2 50-pin single-ended
- Ethernet RJ45
- VGA 15-pin Dsub graphics connector
- Two PS/2 connectors for keyboard/mouse
- Audio (microphone, headphones, line-in)
- 15-pin connector for external floppy
- High-pin-count connector for docking station
- Connector for an special I/O breakout cable to connect:
  - Two Serial RS232C DB9
  - Parallel DB25
  - AUI 10 Mbit Ethernet

3.54.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- NetBSD
- OpenBSD

Not all devices or expansion options and modules are supported in Linux and the BSDs. OpenBSD fully supports the Cardbus controller and a range of different Cardbus and PCMCIA devices (Fast-Ethernet, WLAN etc.).

3.54.5 Benchmarks

Model	SPEC95, int	SPEC95, fp
PrecisionBook 132	6.49	6.54
PrecisionBook 160	7.78	7.39
PrecisionBook 180	9.22	9.43

3.54.6 References

- PrecisionBook hardware reference guide (Tadpole RDI)

- PrecisionBook user guide (Tadpole RDI)
- RDI software for HP-UX 10.20 installation guide (Tadpole RDI)
- RDI software release notes (Tadpole RDI)
- PrecisionBook Technical White Paper (Tadpole RDI: August 1999)
- ADTX SCSI-IDE converters information from Michael Shalayeff

3.55 SAIC Galaxy 1100

3.55.1 Overview

The SAIC Galaxy 1100 were portable PA-RISC workstations based on the HP 9000/712 workstation in a ruggedized case released in 1994. They were not "notebooks" in the current sense but portable workstations — without battery needing standard AC power. Since the Galaxy were normal PA-RISC workstations they supported standard PA-RISC operating systems and applications.

The Galaxy 1100 portables are very rare, originally built for military and intelligence applications in 1994. HP PA-RISC computers were part of the US Navy TAC-4 program through which HP supplied HP 9000 PA-RISC workstations used throughout the US Navy for measurement and control. For harsher environments where standard workstations were not robust enough, HP contracted with SAIC to produce a ruggedized MIL-SPEC portable workstation — the SAIC Galaxy 1100 based on the HP 9000 712.

- Portable requirements: Navy TAC-4
- Shock: Federal Test Method Standard 101C, Method 5007.1 free-fall drop test
- Airborne: MIL-STD-740-1, Grade C, Table 1

SAIC developed several specialzed I/O devices for the Galaxy system that attached to the GIO/TSIO expansion slots. As these systems were produced under a military contract and sometimes used in classified environment only few became available to civilian world. There were only two other portable PA-RISC computers produced — the RDI PrecisionBook, based on HP Visualize C132L, and the Japanese Hitachi 3050RX/100C.

3.55.2 System

CPU

- PA-7100LC 60 MHz with 1 KB on-chip L1 and 64 KB off-chip L1 cache
- PA-7100LC 80 MHz with 1 KB on-chip L1 and 256 KB off-chip L1 cache

Chipset

- LASI chipset
- NCR 53C710 8-bit single-ended SCSI-2
- Intel 82596CA 10 Mbit Ethernet controller
- Harmony CD/DAT quality 16-bit stereo audio
- Artist graphics, 8-bit
- Other I/O (serial, parallel, Floppy)
- PCMCIA controller

Display

- 10.4âĂş active matrix LCD
- XGA resolution, *i.e.*, 1024×768
- 256 colors (8-bit color depth)
- 60Hz refresh

Human Input

- PS/2-compatible, 84-key integrated QWERTY keyboard with 12 function keys
- Trackball and three-button pad

Buses

- GSC system level I/O bus
- SCSI-2 Fast-Narrow single-ended bus

Memory

- 72-pin ECC SIMMs, same as on standard HP 9000 712
- (Original documentation describes proprietary memory modules)
- 8-32 MB modules
- Four sockets
- 16 MB (2×8) minimum, 128 MB (4×32) maximum
- Memory has to be installed in pairs, starting from slot 0

Expansion

- Two PCMCIA slots, for either two Type I/II or one Type III PCMCIA card
- Proprietary SAIC modules for the standard GIO/TSIO slots

Drives

- One 3.5âĂş Fast-Narrow 50-pin SCSI-2 hard drive
- One 3.5âĂş 1.44 MB Floppy drive

3.55.3 External

- SCSI-2 50-pin Fast-Narrow single-ended
- Serial RS232C DB9 (up to 115200 baud)
- Parallel DB25
- Ethernet RJ45
- Ethernet AUI 15-pin
- VGA HD15
- Two PS/2 connectors for keyboard & mouse
- Three phone jacks (microphone, headphones and line-in)

3.55.4 Operating systems

- HP-UX10.20, 11.00 and 11i v1
- Linux
- NetBSD
- OpenBSD

3.55.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
Galaxy 1100 80 MHz	99	122	3.12	3.55

3.55.6 Dimensions

Height	Width	Depth	Weight
114mm	412mm	311mm	8kg

3.55.7 References

- SAIC Galaxy 1100 product page (archive.org mirror), Old product page with photos and details on the SAIC. Science Applications International Corporation (1996). Archive.org mirror accessed 2 Oct 2007
- RISCy BUSINESS presents the SAIC GALAXY 1100 (Accessed 2019)

3.56 Stratus Continuum

Stratus Technologies produced a line of "Ultra High Availability Fault Tolerant" PA-RISC servers, called Continuum, in the 1990s. The Continuum were based on different PA-RISC processors and sold as the Continuum 400, 600 and 1200 series between 1995 and 2004. These systems feature a great deal of redundancy, with up to four CPUs to form one single logical processor.

The PA-RISC-powered systems were phased out in the mid-2000s in favor of Intel-based systems, the Xeon Pentium 4 based ftServer V Series.

Earlier Stratus computers used different architectures — the Stratus/32, XA400 and XA2000 from the 1980s used Motorola MC680x0 processors, the XA/R from the early-1990s utilized multiprocessor Intel i860 (!) RISC processors.

Thanks to Ti Kan (2004) for the input.

3.56.1 Continuum 400

The Continuum 400 series has the same CPU/memory architecture as the 600/1200, but the I/O bus is different. Instead of a Golf bus, it has an **X** bus that connects each CPU/memory module to a pair of PCI bridge boards. All I/O connectivity is via PCI cards. There are two PCI bays of 7 slots each, connected downstream from the PCI bridge boards. Each bay has a dual channel SCSI adapter on it as standard equipment. These are also cross-wired and dual-initiated much in the same way as the SCSI ports on the 600/1200 systems. The 400 is also typically shipped with a pair of Ethernet adapter cards. The PCI bridge boards also each contains a removable PCMCIA flash memory card. This is used as the boot device. FTX puts the bootloader as well as the UNIX kernel on there, whereas HP-UX only uses it for the bootloader.

The PCI bay doors control the power the the PCI slots. Once opened, all slots in that bay are powered off to facilitate removal and insertion of cards. The system continues to run on cards in the other bay. An interlock mechanism prevents both bay doors from being opened at the same time.

Two chassis versions were available, one a short form-factor AC-powered, the other a tall CO central office version with a choice of AC or DC power.

The Continuum 400 supported mainly Stratus-modified HP-UX as operating systems, with Stratus own FTX Unix only sold exceptionally.

3.56.2 Continuum 600 and 1200

The Continuum 600 and 1200 series are similar designs but with different chassis configuration. The 600 has six slots for the main Golf bus, and the rest of the space is filled with I/O card cages meant for secondary I/O boards. The 1200 has twelve slots for the main bus which occupies the entire width of the chassis. Secondary I/O boards go into a separate chassis. Both models have space for two rows of cooling fans on the top, and two rows of disk drives on the bottom and also either a QIC or DAT tape drive or CDROM drive. The redundant power supplies with built-in UPS resides at the very bottom.

The main Golf bus is the main interconnect between the "big" boards:

- G7xx - CPU and memory boards
- K450 - 4-channel HVD fast wide SCSI and Ethernet adapter

- K460 - 4-channel HVD fast wide SCSI and Ethernet adapter
- K470 - A "carrier board" for PMC PCI-mezzanine daughter cards
- K600 - Adapter to the secondary I/O card cages

On the 600 chassis, the six slots consists of two for the pair or CPU/memory boards, and four more slots for two pairs of "big" boards. On the 1200 chassis, there are slots for two pairs of CPU/memory boards and four pairs of big boards.

In addition the 600/1200 main chassis also has a pair of Console Controller cards which provides the RS232 console terminal and RSN modem connectivity. This controller also has a command mode that allows the operator to type commands on the console to reset the system, power down, power up, etc. It runs on "housekeeping power" that is independent of the rest of the system. The Console controller also contains some environmental monitoring circuitry that checks the chassis internal temperature and will increase the cooling fan speed if necessary.

The secondary I/O chassis can be used to plug in a wide array of I/O boards, all Stratus proprietary. These boards are also used on the XA/R line. FTX supported many of the communications boards like ISDN, serial, parallel, X.25, and all sorts of other comm boards. HP-UX did not support many of those, if any. VOS also supported disk and tape I/O through this.

The Continuum 600 and 1200 were geared towards the VOS transactional operating system from Stratus, with FTX Unix offered only exceptionally.

3.56.3 Processors and architecture

Each logical processor is physically two pairs of actual CPUs, that means four physical CPU chips per single logical one. Each pair is located on a separate FRU. All processors run "lock-stepped," they do exactly the same thing at the same time. Comparator logic between each two physical CPU pair monitors for discrepancies. If any physical CPU glitches or does something different, the comparator logic will detect the error and take that pair of CPUs offline, while the system continues to run on the other pair. There is no "failover time." On multi-processor boards, each FRU contains multiple pairs of the logical processor halves.

The memory is self-checking and ECC corrected. If an uncorrectable error occurs, the FRU in which the memory is located will also be taken offline.

The big I/O boards are also self-checking and contain a pair of everything. However, with the exception of the K600 they do not run lock-stepped to the twin FRU. For example on the K450/K460 boards, each of the SCSI host adapters is connected via the backplane into the same SCSI bus on the partner board, but each board's controller occupies a different SCSI target ID. Only one controller is normally active, but when a failure occurs on the active board, all I/O is switched to the other controller. For the Ethernet ports on that board, they can be wired up to the same network or to different networks, and a software RNI redundant network interface layer provides transparent switching. All disks are mirrored.

3.56.4 Operating systems

Operating system support was split between the Continuum 400 on the one hand and the Continuum 600 and 1200 on the other hand.

Continuum 400: Marketed and offered commercially with Stratus-modified **HP-UX** Unix 11.00 as main choice. The Continuum 400 also supported Stratus' own **FTX Unix**, which was only sold on an exceptional basis. There also was a cancelled effort to port the Stratus VOS operating system to the 400s. Continuum 400 servers running the Stratus-modified HP-UX 11.00 were fully binary compatible with stock HP HP-UX — programs compiled for "normal" HP-UX ran without changes on Continuum 400.

Continuum 600 and 1200: These were sold primarily with **Stratus VOS**, geared towards transaction processing, with releases 13.0 (1995) to 14.7.2 (2005) on PA-RISC hardware. Also offered on the 600s and 1200s on an exceptional basis was **Stratus FTX**, System V Unix from Stratus. Hardware support was limited though.

3.56.5 System Table

Table 3.133: Stratus Continuum PA-RISC servers overview

Model	CPU	Logical physical CPUs	Cache per CPU	RAM max	Expansion max	Storage max	I/O max	OS
419	PA-8500 360 MHz	L1/P4	1.5 MB	8 GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100 Mbit, 8 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
429	PA-8500 360 MHz	L2/P8	1.5 MB	8 GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100 Mbit, 8 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
439	PA-8600 480 MHz	L1/P4	1.5 MB	8 GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100 Mbit, 32 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
449	PA-8600 480 MHz	L2/P8	1.5 MB	8 GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape drives	16 10/100 Mbit, 32 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX, FTX
610S	PA-7100 72 MHz	L1/P4	512 KB	128 MB	6 slots			VOS, FTX
610	PA-7100 72 MHz	L1/P4	512 KB	512 MB	6 slots			VOS, FTX
615S	PA-7100 96 MHz	L1/P4	2 MB	128 MB	6 slots			VOS, FTX

615	PA-7100 96 MHz	L1/P4	2 MB	1 GB	6 slots			VOS, FTX
616S	PA-8500 360 MHz	L1/P4	1.5 MB	0.5 GB	6 slots			VOS, FTX
616	PA-8500 360 MHz	L1/P4	1.5 MB	2 GB	6 PCI, 2 Stratus I/O, 28 I/O	L47/P94 disks, 4 tape drives	10 10/100 Mbit, 8 T1/E1, 8 TR, 4 FDDI, 448 Async, 112 RS232, 28 X.21, 56 V.35	VOS, FTX
618	PA-8000 180 MHz	L1/P4	2 MB	3 GB	6 slots			VOS, FTX
619	PA-8500 380 MHz	L1/P4	1.5 MB	4 GB	6 slots			VOS, FTX
620	PA-7100 72 MHz	L2/P8	512 KB	512 MB	6 slots			VOS, FTX
625	PA-7100 96 MHz	L2/P8	2 MB	2 GB	6 slots			VOS, FTX
628	PA-8000 180 MHz	L2/P8	2 MB	3 GB	6 slots			VOS, FTX
629	PA-8500 380 MHz	L2/P8	1.5 MB	4 GB	6 slots			VOS, FTX
651-2	PA-8600 480 MHz	L1/P4	1.5 MB	4 GB	6 PCI, 2 Stratus I/O, 28 I/O	L47/P94 disks, 4 tape drives	10 10/100 Mbit, 8 T1/E1, 8 TR, 4 FDDI, 448 Async, 112 RS232, 28 X.21, 56 V.35	VOS, FTX

652-2	PA-8600 480 MHz	L2/P8	1.5 MB	4 GB	6 PCI, 2 Stratus I/O, 28 I/O	L47/P94 disks, 4 tape drives	10 10/100 Mbit, 8 T1/E1, 8 TR, 4 FDDI, 448 Async, 112 RS232, 28 X.21, 56 V.35	VOS, FTX
1210	PA-7100 72 MHz	L1/P4	512 KB	?	12 slots			VOS, FTX
1215	PA-7100 96 MHz	L1/P4	2 MB	?	12 slots			VOS, FTX
1218	PA-8000 180 MHz	L1/P4	2 MB	3 GB	12 slots			VOS, FTX
1219	PA-8500 380 MHz	L1/P4	1.5 MB	4 GB	12 slots			VOS, FTX
1220	PA-7100 72 MHz	L2/P8	512 KB	512 MB	12 slots			VOS, FTX
1225	PA-7100 96 MHz	L2/P8	2 MB	2 GB	12 slots			VOS, FTX
1228	PA-8000 180 MHz	L2/P8	2 MB	3 GB	12 slots			VOS, FTX
1229	PA-8500 380 MHz	L2/P8	1.5 MB	4 GB	12 slots			VOS, FTX
1245	PA-7100 96 MHz	L4/P16	2 MB	2 GB	12 slots			VOS, FTX
1251-2	PA-8600 480 MHz	L1/P4	1.5 MB	4 GB	18 PCI, 6 Stratus I/O, 84 I/O	L95/P190 disks, 4 tape drives	18 10/100 Mbit, 8 T1/E1, 24 TR, 8 FDDI, 448 Async, 112 RS232, 84 X.21, 168 V.35	VOS, FTX

1252-2	PA-8600 480 MHz	L2/P8	1.5 MB	4 GB	18 PCI, 6 Stratus I/O, 84 I/O	L95/P190 disks, 4 tape drives	18 10/100 Mbit, 8 T1/E1, 24 TR, 8 FDDI, 448 Async, 112 RS232, 84 X.21, 168 V.35	VOS, FTX

- **Logical/Physical CPUs**: "**L**" and "**P**" denote **L***ogical* and **P***hysical* devices — logical CPUs are made up of two pairs of CPUs each (*i.e.*, 2×2)
- **Storage**: "**L**" and "**P**" denote **L***ogical* and **P***hysical* devices — logical disk drives are formed from physical devices via RAID sets
- **I/O**: Maximum number of I/O devices supported (not necessarily always configured with this number); notably the devices are also redundant

3.56.6 References

- The Stratus Continuum Family (URL gone)
- The Stratus Continuum 400 Series (URL gone)
- The Stratus Continuum 600 and 1200 Series (URL gone)
- Stratus Machine History (August 2017: Paul Green. Accessed March 2021)
- Stratus Continuum Series - VOS, Stratus Virtual Operating system (URL gone)
- Continuum 600/1200 Series (PA-7100) Service Announcement (URL gone)

Further reading

- Stratus Shifts High-End Servers From PA-RISC to Intel, Computer World 2004

3.57 PA-RISC Third Party Systems

3.57.1 Overview

Several other vendors sold PA-RISC workstations and servers in the mid-1990s as part of the Precision RISC Organisation (PRO) from HP. Hitachi, Mitsubishi, NEC and Oki were active at that timeframe with various PA-RISC offerings on the Japanese market. Some of the third party PA-RISC computers sold by PRO members as OEM in their markets during the mid-1990s were:

- Hitachi sold both indigenous workstations (3050RX) and servers (3500) with PA-RISC processors, and relabeled systems from HP as OEM (9000V). The Hitachi page has been updated to include information on more 3050RX workstations, 3500 servers and the OEM systems.
- Mitsubishi limited its PA-RISC line to the original HP 9000 "Snakes" (720, 730 and 750) sold in the early-1990s as "MELCOM ME RISC series"
- NEC sold a range of HP PA-RISC servers as OEM, mostly K, D, a L-Class
- OKI offered almost the whole range of HP PA-RISC servers and workstations in the 1990s with the various "OKITAC 9000 series."
- Samsung apparently also sold some rebadged HP 9000 700 workstations in Korea

3.57.2 Hitachi

Hitachi produced several lines of computers with PA-RISC processors during the 1990s, including Hitachi-designed workstations (3050RX) and servers (3500), which run Hitachi's HP-UX variant — HI-UX/WE2 (apparently compatible). Hitachi also sold various OEM systems from HP in Japan, rebranded as Hitachi 9000V.

Hitachi 3050RX workstations

These PA-RISC workstations from the mid-1990s were pretty rare systems exclusive to Japan, apparently marketed as "Hitachi Creative Station 3050RX Group" .

Model	CPU	Caches	RAM max.	Expansion	Notes
3050RX/100C	Hitachi PA/50L 33 MHz	8/4 KB	80 MB	?	Color laptop, 1024x768 TFT LCD
3050RX/200	Hitachi PA/50M 33 MHz	8/4 KB	144 MB	?	Low-cost low-power model
3050RX/220	PA-7100 50 MHz	64/64 KB	192 MB	none	
3050RX/220	PA-7100LC 60 MHz	256 KB	?	?	
3050RX/230	PA-7100 80 MHz	256/256 KB	192 MB	none	
3050RX/235	PA-7100LC 80 MHz	512 KB	?	?	
3050RX/255	PA-7300LC 132 MHz	64/64 KB L1 (1 MB L2)	256 MB	Two slots	

3050RX/310S	PA-7100 33/40 MHz	64/64 KB L1	272 MB	One slot	
3050RX/320	PA-7100 50 MHz	64/64 KB L1	416 MB	Three slots	
3050RX/320G	PA-7100 50 MHz	64/64 KB L1	192 MB	Three slots	
3050RX/320S	PA-7100 50 MHz	64/64 KB L1	272 MB	One slot	
3050RX/330	PA-7100 80 MHz	256/256 KB	416 MB	Three slots	
3050RX/330G	PA-7100 80 MHz	256/256 KB	192 MB	Three slots	
3050RX/330T	PA-7100 80 MHz	256/256 KB	192 MB	Three slots	
3050RX/330	PA-7100 100 MHz	256/256 KB L1	416 MB	Three slots	
3050RX/355E	PA-7300LC 132 MHz	64/64 KB L1 (1 MB L2)	1.5 GB	Two slots one audio	
3050RX/365	PA-7300LC 160 MHz	64/64 KB L1 (1 MB L2)	1.5 GB	Two slots one audio	
3050RX/430	PA-7100 80 MHz	256/256 KB L1	768 MB	Seven slots	
3050RX/440	PA-7100 100 MHz	256/256 KB L1	768 MB	Seven slots	
3050RX/535	PA-7100LC 80 MHz	512 KB L1	?	?	

Hitachi 3500 servers

Model	CPU	Cache (I/D)	RAM(max.)	Expansion
3500/310	PA-7100 50 MHz	64/64 KB	416 MB	?
3500/410	PA-7100 50 MHz	64/64 KB	512 MB	?
3500/510	PA-7100 50 MHz	64/64 KB	512 MB	?
3500/520	PA-7100 50 MHz	256/256 KB	512 MB	?
3500/530	PA-7100 80 MHz	256/256 KB	512 MB	?
3500/540	PA-7100100 MHz	256/256 KB	512 MB	?
3500/630	PA-7100 80 MHz	256/256 KB	1024 MB	?
3500/640	PA-7100100 MHz	256/256 KB	1024 MB	?

Hitachi 9000V OEM systems

Hitachi also sold a line of original HP systems as OEM (probably only in Japan) — rebranded as "Hitachi 9000V series" which included the following systems from 1995 onwards:

Model	HP equivalent
9000V V715/100XC, V715/100, V715/80, V715/64	HP 9000/715 (newer models)
9000V V715/100Tiny, V715/80Tiny	HP 9000/712 (probably)
9000V V735/125	HP 9000 735/125
9000V VE55, VE45, VE35, VE25	HP 9000/E-Class
9000V VQ200, VQ210	HP 9000/J200, HP 9000/J210
9000V VR100, VR200, VR400	HP 9000/K100, HP 9000/K200, HP 9000/K400

9000V VT500	HP 9000/T500 (T-Class)

References

◈ IPSJ Computer Museum: 3050RX Hitachi Group/3500 Series [Google translation into English] Information Processing Society of Japan (n.d. Accessed August 2008) and

3.57.3 Mitsubishi

Mitsubishi Electric of Japan sold rebranded HP 9000 workstations in the early 1990s as OEM under the name "MELCOM ME RISC series," as part of the PRO. Apparently only three models were sold (the original HP 9000 "snakes" workstations):

Model	HP equivalent
ME/R7200 and ME/S7200	HP 9000/720
ME/R7300 and ME/S7300	HP 9000/730
ME/R7500 and ME/S7500	HP 9000/750

3.57.4 NEC

NEC Electronics of Japan sold a range of HP PA-RISC servers as OEM, mostly in Japan:

Model	HP equivalent
TX7/K370	HP 9000 K-Class
TX7/D280	HP 9000 D-Class
NX7000/L1000, L2000, L3000	HP 9000 L1000, HP 9000 L2000, HP 9000 L3000
TX7/P590	Custom NEC system based on up to eight PA-8000 processors
TX7/V2200	HP 9000/V2200

3.57.5 OKI

Similar to Mitsubishi in the early 1990s, Oki Electric Industry sold various PA-RISC workstations and servers from HP rebranded as OEM systems. These were integrated the "OKITAC" brand and shipped from 1992 onward:

Model	HP equivalent
OKITAC 9000/800 Series	HP 9000/800 Nova servers
OKITAC 9000 A Series	HP 9000/A180C
OKITAC 9000 B Series	HP Visualize B1000
OKITAC 9000 C Series	HP Visualize C3000
OKITAC 9000 D Series	HP 9000 D-Class
OKITAC 9000 J Series	HP Visualize J5000
OKITAC 9000 K Series	HP 9000 K-Class
OKITAC 9000 R Series	HP 9000 R380 and R390

3.57.6 Samsung

Samsung Electronics Co apparently also produced and sold HP 9000 workstations under licence from 1993 on, as part of the Precision RISC Organization, PRO. The following systems were designed by the Samsung Workstation Division in San Jose, running "SS-UX" operating system, with added "I/O-features" to standard HP-UX Unix.

- **SWS715**: with PA-7100 at 50 and 33 MHz
- Both are probably OEM clones of the HP 9000 715 workstations

3.57.7 References

- HITACHI CLAIMS TO HAVE THE INDUSTRYÃćâĆňâĎćs CHEAPEST UNIX WORKSTATION, USING PRECISION ARCHITECTURE..., CBR Online Archive, 28 Oct 1993
- October 1993 PROgress Newsletter, USENET post, Google Archive, 11/01/1993
- SAMSUNG, WITH FIRST PA-RISC STATION, COMMITS TO NT CBR Online Archive, 21 Mar 1993

3.58 PA-RISC Timeline from 1982

This page details the timeline from the mid-1980s on for both HP 9000 PA-RISC computers and the Unix-centric PA-RISC operating systems. For the hardware platform, history starts in the early 1980s with the HP FOCUS predecessors of PA-RISC. The software timeline starts in the late 1980s in parallel to first commercial PA-RISC products. There is a dedicated article on the History of the HP 9000 PA-RISC Series.

3.58.1 HP 9000 Computers

Below are the release years of PA-RISC processors and computer systems. The data is not complete, especially for entries from the 2000s and there are often discrepancies between announcements, release dates and actual shipped systems.

Table 3.140: PA-RISC hardware timeline

Year	CPU	Workstation	Server	Mainframe	Other
1982	FOCUS	*520*	*530*, *540*		
1983					
1984			*550*		
1985					
1986	TS-1			840	
1987	NS-1		825	850	
1988			835		
1989	NS-2 PCX		808, 815 845 822, 832	860	
1990			842, 852	855, 870	
1991	PA-7000	*720*, *730*, *750*	865 F10, F20, F30 H20, H30, H40 I30, I40		
1992	PA-7100	*705*, *710* *715/33*, *50*, *75* *725*, *735*, *755*	G50, H50, I50	890	*742i*, *745i* *747i*
1993			G60, G70 H60, H70 I60, I70		
1994	PA-7100LC	*712/60*, 80 *715/64*, 80, 100 SAIC Galaxy 1100	E25, E35, E45	T500 SPP1000	*743i* *748i*
1995	PA-7200	*712/100* *715/100XC* C100, C110 J200, J210	E55, K100 K200, K210 K400, K410	T520 SPP1200	
1996	PA-7300LC PA-8000	B132L, B160L C160L C160, C180 J280	D200, D300 D210, D310 D260, D360 D270, D370 K250, K260 K450, K460	SPP1600	*744*, *748*

1997	PA-8200	B180L C200, C240 J282, J2240	D220, D320 D230, D330 D280, D380 K370, K570	T600 S-Class, X-Class SPP2000 V2200	
1998	PA-8500	RDI Precision-Book	A180 R380, R390 K380, K580	V2250	*745*
1999		C360, C3000 B1000 J5000, J7000	L1000, L2000 rp5430, rp5450 N4000	V2500	
2000	PA-8600	B2000, B2600 C3600 J5600, J6000	A400, A500 rp2400, rp2430 rp2450, rp2470 L1500, L3000 rp5430, rp5470	V2600	
2001	PA-8700 *Merced*	C3650, C3700 J6700 *i2000*	rp7400		
2002	*McKinley*	*zx2000*	rp2405, rp5405 rp7405, rp7410		
2003	*Madison* *Deerfield*		*rx2600* *rx5670*		
2004	PA-8800 *Hondo*	c8000	rp3410, rp3440 rp4410, rp4440 *rx1600, rx1620* *rx2620, rx4640*		
2005	PA-8900				
2006	*Montecito*				
2007	*Montvale*		*rx2660*		
2008					
2009					
2010	*Tukwila*				
2011					
2012	*Poulson*				

3.58.2 Operating systems

The History of PA-RISC Operating Systems starts in the late 1980s, with both commercial as well as research products. Below are the approximate release years of several of the major PA-RISC operating systems. Data might be incomplete, especially the information from post HP-UX 11i v3 and associated versions.

Table 3.141: PA-RISC operating systems timeline

Year	HP	Mach	BSD	Linux	Other
1988					HP Tut
1989	HP-UX 5.3, HP-UX 7.0		Utah HPBSD		HP Tut
1990		HP OSF/1	Utah HPBSD		Chorus (835)
1991	HP-UX 8.0	Utah Mach 3/UX HP OSF/1			Chorus (720)
1992	HP-UX 9.0				
1993			Utah HPBSD 2.0		

1994		Utah Mach 4/Lites OSF MK-PA 6.0 NeXTSTEP 3.3			
1995	HP-UX 10.00	OSF MK-PA 6.3			
1996	HP-UX 10.10, 10.20	Utah Mach 4/Lites II OSF MK-PA 7.x			
1997	HP-UX 10.30, 11.00			OSF MkLinux	
1998				PA-RISC Linux OSF MkLinux	
1999			OpenBSD	PA-RISC Linux	
2000	HP-UX 11.10, 11i v1 (11.11)				
2001	HP-UX 11i v1.5 (11.20)				
2002	HP-UX 11i v1.6 (11.22)			Debian 3.0	
2003			OpenBSD 3.3		
2004			OpenBSD 3.5, 3.6 (NetBSD 2.0)		
2005	HP-UX 11i v2 (11.23)		OpenBSD 3.7, 3.8 NetBSD 3.0	Debian 3.1 Gentoo 2005.1	
2006			OpenBSD 3.9, 4.0 NetBSD 3.1		
2007	HP-UX 11i v3 (11.31)		OpenBSD 4.1, 4.2 NetBSD 4.0	Debian 4.0 Gentoo 2007.0	
2008			OpenBSD 4.3, 4.4	Gentoo 2008.0	
2009			OpenBSD 4.5, 4.6 NetBSD 5.0	Debian 5.0	
2010			OpenBSD 4.7, 4.8 NetBSD 5.1		
2011			OpenBSD 4.9, 5.0	Debian Ports	
2012			OpenBSD 5.1, 5.2 NetBSD 5.2, 6.0		
2013			OpenBSD 5.3, 5.4 NetBSD 6.1		
2014			OpenBSD 5.5, 5.6		
2015			OpenBSD 5.7, 5.8 NetBSD 7.0		
2016			OpenBSD 5.9, 6.0		

2017			OpenBSD 6.1, 6.2 NetBSD 7.1		

3.58.3 Historic prices

Collection of the historic prices of PA-RISC computers, around the date of introduction. These are indicative prices which have been collected over the years from a variety of sources, such as press releases, articles, journals. The data is not based on official or coherent sources and as such only indicative. There are probable contradictions and inaccuracies, but most of it was included here to preserve some information from that time. Many of the original sources are disappearing from the web, which includes 1990s press releases, articles in journals and magazines and marketing material. HP changed prices and especially packaging of systems a lot due to market pressures, such as Windows NT workstations for technical computing, as well as marketing reasons.

Table 3.142: PA-RISC computers entry dates and pricing

Model	Released	Entry price
520	1982	$30,000
530	1982	$23,105
540	1982	$24,115
550	1984	
705	1992	
710	1992	$7,490
712/60	1994	$4,000
712/80	1994	$8,820
712/100	1995	$15,100
715/33	1992	$4,995
715/50	1992	$11,895
715/64	1994	$10,000
715/75	1992	
715/80	1994	$13,000
715/100	1994	$19,000
715/100XC	1995	$21,000
720	1991	$11,990
725/50	1992	$17,895
725/75	1992	
725/100	1994	
730	1991	
735/99	1992	$37,395
735/125	1992	
742i/50	1992	$8,000
743i/64	1994	$4,355
743i/100	1994	
744/132L	1996	$8,600
744/165L	1997	
745i/50	1992	$13,390
745i/100	1992	
745/132L	1998	$9,999
745/165L	1998	

747i/50	1992	$15,990
747i/100	1992	
748i/64	1994	
748i/100	1994	
748/132L	1996	$12,000
748/165L	1996	
750	1991	$118,190
755/99	1992	$58,995
755/125	1992	
SAIC Galaxy 1100	1994	
RDI PrecisionBook 132	1998	$11,995
RDI PrecisionBook 160	1998	$14,995
RDI PrecisionBook 180	1998	
808	1989	
815	1989	$14,900
822	1989	$19,950
825	1987	$42,500
832	1989	$30,000
835	1988	$45,000
840	1986	$113,500
842	1990	$85,000
845	1989	
850	1987	$200,000
852	1990	$143,000
855	1990	$300,000
860	1989	
865	1991	$275,000
870/300	1990	$440,000 (/300)$530,000 (/400)
890	1992	
A180	1998	
A180C	1998	$16,000
A400	2000	$4,600
A500	2000	$9,200
B132L	1996	$8,00
B160L	1996	
B180L	1997	$16,500
B1000	1999	$9,900
B2000	2000	
B2600	2000	
C100	1995	$19,715
C110	1995	$25,715
C132L	1996	
C160L	1996	$19,480
C160	1996	
C180	1996	
C200	1997	$21,000
C240	1997	$46,000
C360	1998	$22,365
C3000	1999	$13,800

C3600	2000	
C3650	2001	
C3700	2001	
C3750	2001	
C8000	2004	
D200	1996	
D210	1996	$6,900
D220	1997	$8,900
D230	1997	
D250	1996	
D260	1996	
D270	1996	$22,260
D280	1997	$25,450
D300	1996	
D310	1996	
D320	1997	
D330	1997	$16,700
D350	1996	
D360	1996	
D370	1996	$25,250
D380	1997	$30,490
D390	1998	
E25 (806)	1994	$6,000
E35 (816)	1994	
E45 (826)	1994	$11,320
E55 (856)	1995	
F10 (807)	1991	$12,895
F20 (807)	1991	$20,000
F30 (837)	1991	
H20 (827)	1991	
G30/H30 (847)	1991	$65,000
G40/H40 (867)	1991	$112,500
G50/H50 (887)	1992	
G60/H60 (887)	1993	
G70/H70 (887)	1993	
I30 (857)	1991	$95,000
I40 (877)	1991	$140,000
I50 (897)	1992	
I60 (897)	1993	
I70 (897)	1993	
i2000	2001	$7,000
J200	1995	
J210	1995	
J210XC	1995	
J280	1996	$38,520
J282	1997	
J2240	1997	$55,900
J5000	1999	$22,700
J5600	2000	

J6000	2000	
J6700	2001	
J6750	2001	
J7000	1999	
J7600	2000	
K100	1995	
K200	1995	
K210	1995	$40,000
K220	1996	
K250	1996	$52,200
K260	1996	$77,200
K370	1997	$66,500
K380	1998	
K400	1995	
K410	1995	$65,000
K420	1996	
K450	1996	
K460	1996	
K570	1997	$86,500
K580	1998	
L1000	1999	$16,000
L1500	2000	
L2000	1999	$21,500
L3000	2000	$39,000
N4000	1999	$48,000
R380	1998	$17,350
R390	1998	
rp2400	2000	
rp2405	2002	
rp2430	2000	
rp2450	2000	
rp2470	2000	
rp3410	2004	$4,000
rp3440	2004	$7,000
rp4410	2004	
rp4440	2004	$21,000
rp5400	1999	$16,000
rp5405	2002	$29,026
rp5430	2000	$39,000
rp5450	1999	$21,500
rp5470	2000	
rp7400	2001	
rp7405	2002	$50,595
rp7410	2002	$92,250
rx1600	2004	$3,000
rx1620	2004	$4,000
rx2600	2003	$7,300
rx2620	2004	
rx4610	2001	$25,000

rx4640	2004	$15,000
rx5670	2003	$27,000
SPP1000/CD	1994	$145,000
SPP1000/XA	1994	$550,000
SPP1200/CD	1995	$160,000
SPP1200/XA	1995	$586,000
SPP1600	1996	
SPP2000 S-Class	1997	$189,000
SPP2000 X-Class	1997	$720,000 (min) $3M (max)
T500	1993	$165,000 uni $660,000 12-way
T520	1995	$145,000 uni $520,000 14-way
T600	1997	
V2200	1997	$157,000
V2250	1998	
V2500	1999	
V2600	2000	
zx2000	2002	$3,300
zx6000	2002	$4,900
16600A	1997	$24,240
16700A	1997	$9,900
16701A	1997	$5,000

Chapter 4

PA-RISC Operating Systems

4.1 Overview

A broad range of operating systems has been available over the years for PA-RISC workstations and servers. Most of them are either commercial Unix or Unix-like derivates and open source projects, with different designs having both been ported to and developed specifically for PA-RISC. A separate article is dedicated to the history of PA-RISC operating systems.

Commercial

- **HP-UX**: is HP's main commercial Unix operating system for its PA-RISC workstations and servers. The popular HP-UX 10.20 from 1996 has the widest support for HP 9000 700 workstations and HP 9000 800 servers, HP-UX 11i from the 2000s runs on most PA-RISC 1.1, 2.0 and Itanium 2 computers from HP.
- **NeXTSTEP**: NeXTSTEP on PA-RISC was a commercial Mach-based operating system from the 1990s with an Unix userland and a then extremely modern GUI, ported to PA-RISC in 1994. Support for some 32-bit PA-RISC machines was available in Version 3.3, with limited hardware support.
- **MPE/iX**, a business real-time operating system for HP 3000 mainframes running PA-RISC. For more information read the 3000-MPE (Software) article from hpmuseum.net and The History of the HP 3000 from Bob Green.
- **HP-RT** , a real-time operating system for HP 9000 740 VME workstations that apparently was based on LynxOS.
- **Convex SPP/UX**, a heavily modified Mach-based operating system for the Convex/HP Exemplar SPP1000, 1200 and 1600 mainframes.
- **Stratus FTX**, System V Unix, and **Stratos VOS**, a transaction-processing oriented system, for the fault-tolerant Continuum servers from Stratus

Open source

- **Linux**: PA-RISC support was included in the mainstream Linux kernels during the 2000s and shipped with Debian and Gentoo distributions as official ports. During the 2010s support declined and development was scaled back.
- **OpenBSD/hppa** is an open source BSD Unix-like operating system ported to HP PA-RISC computers focused on 32-bit workstations and some 64-bit models running in 32-bit mode.
- **NetBSD/hppa** is a free, open source Unix-like operating system, and supports PA-RISC computers since around 2005, called NetBSD/hp700 until the 7.0 release.

Research

- **MkLinux**: a research project from the mid-1990s by the Open Group/OSF to port a Linux kernel onto a Mach microkernel, based on the MK-PA OSF/1 port to PA-RISC.
- **HPBSD** from the University of Utah which was a late-1980s port of 4.3BSD and later 4.4BSD to early 800s servers and 700s workstations.
- **Mach**: Several ports of the Mach microkernel were done during the early 1990s, with HP Tut porting Mach 2.0 and the University of Utah both Mach 3 and Mach 4.
- **OSF/1**: Porting efforts for OSF/1, the proposed Unix operating system by an alliance of DEC, IBM, HP and others to compete with AT&T's and Sun's System V Unix, started around 1990 by

HP with HP OSF/1 and in the mid-1990s by the OSF RI Open Group Research Institute with several releases of MK-PA.

Support overview

Table 4.1: PA-RISC OS support

OS	7	74	8	A	B	C	D	E	FG	J	K	L	N	R	rp	rx	SD	T	V
HP-UX 9	■	❍	■			❍	❍	■	■	❍	❍							❍	
HP-UX 10.20	■	■	■	❍	❍	■	■	■	■	■	■			■				■	
HP-UX 11.00	❍	❍	■	■	■	■	■	■	■	■	■	❍	❍	■				■	■
HP-UX 11i v1	❍	❍	❍	■	■	■	■	■	❍	■	■	■	■	■	■		■	■	■
HP-UX 11i v2				❍								■	■		■	■	■		
HP-UX 11i v3													■		■	■	■		
Linux	■	■		■	■	■	■	❍		■	■	■		■	❍	❍	❍		
OpenBSD	■	■		❍	■	❍	❍			❍	❍								
NetBSD	■	■		❍	■	❍	❍	❍		❍	❍								
NeXTSTEP	❍																		
Mach 3			❍																
Mach 4	❍																		
MkLinux	❍					❍													
OSF/1	❍																		
MK-PA	■									❍									
HP-BSD	■									❍									

4.2 HP-UX

4.2.1 Overview

HP-UX is HP's commercial Unix operating system for its PA-RISC workstations and servers. First released during the 1980s for the earliest PA-RISC servers and their predecessors, the latest HP-UX in version 11i from the 2000s runs on most PA-RISC 1.1 and 2.0 and Itanium 2 computers from HP.

The popular HP-UX 10.20 version from 1996 had different releases for HP 9000 700 workstations and HP 9000 800 servers, HP-UX 11.00 and later had unified releases for servers and workstations. The 11 line of HP-UX was the first complete 64-bit version with support for the features on PA-8x00 processors.

Until version 9.x HP-UX was BSD Unix influenced and close to HPBSD, from the 10.x releases onward HP-UX became more System V Unix (SVR4) like. HP-UX 10.20 was quite popular, since it ran very smoothly on older systems and had support for most available PA-RISC hardware.

4.2.2 HP-UX 10.20

HP-UX 10.20 was released in 1996, and was the HP Unix release that supported almost all 32-bit PA-RISC workstations and servers. For HP-UX, 10.20 was quite fast on all supported machines with at least 64 MB RAM.

Different releases were made for HP 9000/700 workstations and the HP 9000/800 servers, with most 32-bit HP 9000 models supported. About 300-800 MB of disk space was required, with 64 MB RAM minimum, 128 MB or more better. Most HP 9000 graphics options are supported, as are HP I/O devices and networking adapters found on HP 9000s.

Table 4.2: HP-UX 10.20 supported systems

Class	**Computers**
700s	705, 710, 712, 715, 720, 730, 750, 725, 735, 755
740s VME	742i, 743i, 744, 745i, 745, 747i, 748i, 748
Agilent	HP Agilent 16600A, 16700A, 16700B, 16702A, 16702B
A-Class	A180, A180C
B-Class	B132L, B160L, B132L+, B180L+, B1000, B2000
C-Class	C100, C110,C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600
D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
E-Class	E25, E35, E45, E55
F/G/H/I-Class	F10, F20, H20, F30, G30/H30, I30, G40/H40, I40, G50/H50, I50, G60/H60, I60, G70/H70, I70
J-Class	J200, J210, J280, J282, J2240, J5000, J5600, J6000, J7000
K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
R-Class	R380, R390
T-Class	890, T500, T520, T600
Portables	RDI PrecisionBook, SAIC Galaxy 1100

4.2.3 HP-UX 11.00

Version 11.00 of HP-UX is HP's first Unix with a true 64-bit kernel, but still runs on a number of systems featuring a 32-bit CPU. Most HP 9000/800 servers with at least a PA-7000 are supported, although some expansion devices are not. Official support for HP 9000/700 workstations was only continued for systems with at least a PA-7100LC CPU. Older systems with PA-7100 and PA-7150 processors sometimes also run HP-UX 11.00, but unsupported.

11.00 can run in either 64-bit or 32-bit mode on systems with PA2.0 processors such as the PA-8000 or in 32-bit mode on all PA1.1 processors. It needs a minimum 500 MB to 1 GB of free storage space, with at least 128 MB of RAM; more than 256 MB is much better.

Table 4.3: HP-UX 11.00 supported systems

Class	Computers
700s	712, some 715, some 725,
740s VME	743i, 744, 745, 748i, 748
A-Class	A180, A180C, A400, A500
B-Class	B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
C-Class	C100, C110,C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3700, C3750
D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
E-Class	E25, E35, E45, E55
F/G/H/I-Class	F10, F20, H20, F30, G30/H30, I30, G40/H40, I40, G50/H50, I50, G60/H60, I60, G70/H70, I70
J-Class	J200, J210, J280, J282, J2240, J5000, J5600, J6000, J6700, J6750, J7000
K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
L-Class	L1000, L2000, L1500, L3000 (L1500 unsure)
N-Class	N4000, N4000 (unsure)
R-Class	R380, R390
rp	rp2400, rp2430, rp2405, rp2450, rp2470, rp5400, rp5450, rp5430 (unsure), rp5470, rp7400, rp7405, rp7410
T-Class	T500, T520, T600
V-Class	V2200, V2250, V2500, V2600
Portables	RDI PrecisionBook, SAIC Galaxy 1100

4.2.4 HP-UX 11i

Version 11i is the latest HP-UX release for PA-RISC and Itanium based computers. There are different versions of HP-UX 11i targeting different system families.

- 11i v1 (11.11): 32-bit and 64-bit PA-RISC
- 11i v1.5 and v1.6 (11.20 and 11.22): Itanium and Itanium 2
- 11i v2 (11.23): 64-bit PA-RISC and Itanium 2
- 11i v3 (11.31): newer 64-bit PA-RISC and Itanium 2

HP-UX 11i v1 (11.11)

The original HP-UX 11i release from 2000 supports most 64-bit PA-RISC systems and many older 32-bit servers and workstations. Some even older 32-bit PA-RISC systems were officially unsupported but

could be made to work with some v1 releases. 11i was revised a lot in the next few years.

Table 4.4: HP-UX 11i 11.11 supported systems

Class	Computers
700s	712, some 715, some 725,
740s VME	743i, 744, 745, 748i, 748
A-Class	A180, A180C, A400, A500
B-Class	B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
C-Class	C100, C110,C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3700, C3750C8000
D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
E-Class	E25, E35, E45, E55
J-Class	J200, J210, J280, J282, J2240, J5000, J5600, J6000, J6700, J6750, J7000
K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
L-Class	L1000, L2000, L1500, L3000
N-Class	N4000, N4000
R-Class	R380, R390
rp	rp2400, rp2430, rp2405, rp2450, rp2470, rp3410, rp3440, rp4410, rp4440, rp5400, rp5450, rp5430, rp5470, rp7400, rp7405, rp7410 rp7420, rp7440, rp8400, rp8420, rp8440
Superdome	PA-RISC models
T-Class	T500, T520, T600
V-Class	V2200, V2250, V2500, V2600
Portables	RDI PrecisionBook, SAIC Galaxy 1100

HP-UX 11i v1.5 (11.20) and v1.6 (11.22)

HP-UX 11i v1.5 and v1.6 from 2001/2002 were special versions for the first generation HP Itanium and early Itanium 2 systems.

1.5 supported systems

Class	Computers
i-Class	i2000
rx	rx4610

1.6 supported systems

Class	Computers
i-Class	i2000
rx	rx2600, rx5670
zx	zx2000, zx6000 (both v2 May 2005 last)

The list above might be incomplete.

HP-UX 11i v2 (11.23)

HP-UX 11i v2, released in 2005, supported the later 64-bit PA-RISC servers with **rp**-designations and Itanium 2 servers and workstations. Support for 32-bit PA-RISC 1.1 systems was dropped completely along with many of the 64-bit PA-RISC 2.0 computers with only "lettered" model names (B-Class, C-Class).

Table 4.7: HP-UX 11i v2 (11.23) supported systems

Class	Computers
A-Class	A400, A500
L-Class	L1000, L2000, L1500, L3000
N-Class	N4000, N4000
rp	rp2400, rp2430, rp2405, rp2450, rp2470, rp3410, rp3440, rp4410, rp4440, rp5400, rp5450, rp5430, rp5470, rp7400, rp7405, rp7410 rp7420, rp7440, rp8400, rp8420, rp8440
rx	rx1600, rx1620, rx2600, rx2620, rx2660 rx3600, rx4610 (not sure), rx4640, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640
Superdome	Both PA-RISC and Itanium
zx	zx2000, zx6000

HP-UX 11i v3 (11.31)

HP-UX 11i v2 from 2007 was similar to v2 but supported only the 64-bit PA-RISC servers and Itanium 2 servers. Support for many other models, even with rp-designation was dropped.

Table 4.8: HP-UX 11i v3 (11.31) supported systems

Class	Computers
N-Class	N4000, N4000
rp	rp3410, rp3440, rp4410, rp4440, rp7400, rp7405, rp7410 rp7420, rp7440, rp8400, rp8420, rp8440
rx	rx1600, rx1620, rx2600, rx2620, rx2660 rx3600, rx4640, rx5670, rx6600, rx7620, rx7640, rx8620, rx8640
Superdome	Both PA-RISC and Itanium

4.2.5 References

Most of the documentation and references disappeared during the 2010s from the web.

Software

- Software Porting And Archive Centre for HP-UX, compiled software packages for HP-UX 11
- The Written Word FTP for HP-UX 11.00
- The Written Word FTP for HP-UX 11.11
- The Written Word FTP for HP-UX 11.23
- HP software depot (URL gone)

Documentation

- HP DSPP developer page (URL gone)
- Managing HP-UX Software With SD-UX, Hewlett-Packard Company (November 1997: URL gone)

Manuals

- HP-UX 11i Version 1 Installation and Update Guide: HP Servers and Workstations, Hewlett-Packard Company (June 2004: URL gone. HP part number 5990-7279)
- Installing HP-UX 11.0 and Updating HP-UX 10.x to 11.0: HP 9000 Computers, Hewlett-Packard Company (November 1997: URL gone. HP part number B2355-90153)
- Installing and Updating HP-UX 10.20, ACE and Hardware Extensions: HP 9000 Computers, Hewlett-Packard Company (April 1998: URL gone. HP part number B2355-90173)
- HP-UX manual pages, Hewlett-Packard Development Company (2009: URL gone)

Websites

- HP-UX update matrix, (HP-UX 11.x support for workstations) Hewlett-Packard Development Company (2009: URL gone)
- HP-UX server support matrix, (HP-UX 11.x support for servers) Hewlett-Packard Development Company (November 2008: URL gone)
- HP-UX update matrix (archive.org mirror) (HP-UX 10.20 and 11.x support for workstations) Hewlett-Packard Development Company (2003: accessed March 2009)
- HP-UX version and server model support matrix (archive.org mirror) (HP-UX 11 support for servers) Hewlett-Packard Company (2001: accessed April 2009)
- *Building a Bastion Host Using HP-UX 11*, Kevin Steves (April 2000: Hewlett-Packard Sweden)
- docs.hp.com - Technical documentation, good entry to HP/HP-UX documentation (URL gone)

Release notes

- HP-UX 11i v3 Release Notes (archive.org mirror)
- HP-UX 11i v2 Release Notes (archive.org mirror from 2010. Original: docs.hp.com)
- HP-UX 11i v1.5 Release Notes (archive.org mirror from docs.hp.com)

Other documents

- HP-UX FAQ (comp.sys.hp.hpux FAQ) Ian Springer (February 2008: accessed January 2009)
- INFORMATION ON HP9000 SERVERS AND WORKSTATIONS Hewlett Packard Company (1997 (1999): accessed January 2009)

4.3 PA-RISC Linux

4.3.1 Overview

Linux with its PA-RISC Linux port runs on a broad range of both 32-bit and 64-bit workstations and servers. Most of the HP 9000/700s and B/C/J-Class workstations are supported, both 32-bit based on PA-7x00 processors and 64-bit PA-8x00-based systems. SMP is supported, though not as smooth as on other Linux platforms or HP-UX. PA-RISC Linux runs also on many HP 9000 server systems, although several which use proprietary I/O and CPU/memory combinations are unsupported.

Originally started by "The Puffin Group" in 1998, the port of Linux to HP PA-RISC gained momentum after HP started helping with equipment and more importantly, documentation, in 1999 and quickly superseded the earlier Mach-based MkLinux. Because of HP's assistance, the machines targeted at that time were newer than what other ports like OpenBSD or MkLinux supported, such as the A180, B180 and 64-bit PA 2.0 systems.

4.3.2 Systems supported

Table 4.9: PA-RISC Linux supported systems

Class	**Computers**
700s	705, 710, 712, 715, 720, 730, 750, 725, 735, 755
740s VME	742i, 743i, 744, 745i, 745, 747i, 748i, 748
A-Class	A180, A180CA400, A500
B-Class	B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
C-Class	C100, C110,C132L, C160L, C160, C180, C200, C240, C360, C3000, C3600, C3700, C3750, C8000
D-Class	D210, D220, D230, D250, D270, D280, D310, D320, D330, D350, D370, D380, D390
E-Class	E25, E35, E45, E55 (very limited)
J-Class	J200, J210, J280, J282, J2240, J5000, J5600, J6000, J6700, J6750, J7000, J7600
K-Class	K100, K200, K210, K220, K250, K260, K370, K380, K400, K410, K420, K450, K460, K570, K580
L-Class	L1000, L2000, L3000
N-Class	N4000
R-Class	R380, R390
rp	rp2400, rp2430, rp2405, rp2450, rp2470, rp3410, rp3440, rp5400, rp5450, rp5470, rp7400
Portables	RDI PrecisionBook, SAIC Galaxy 1100

Performance is not quite on par with original HP-UX — 50% being a rough estimate of the relative performance, although the overhead of a complete running HP-UX probably consumes much of this advantage, especially on older systems.

4.3.3 Hardware supported

Most I/O subsystems are supported, including many common PC expansion possibilities. Correct X11 graphical support is limited to a small set of HP adapters via the framebuffer device. As the newer

machines are more similar to standard Intel PCs, support is generally better but still lacking in some areas.

4.3.4 Development

In the late 1990s PA-RISC was the last "big" RISC/Unix architecture without a proper Linux port, besides the limited useful Mach-based MkLinux. This had multiple reasons, including that PA-RISC systems were not widely used in academia with a stronger market share in the technical/industrial space, from which they did no escape for a long time. Another reason was HP only reluctantly releasing technical documentation on their systems to the public, which limited interest in and progress of development efforts.

A function of the confinement to the industry was a limited hobbyist base for PA-RISC as the available machines were not well documented and did not have proper operating systems for private users, as compared to for example the more popular Sun SPARC systems. Slow progress was made in 1999 with the initial start of the original Linux kernel on PA-RISC, as there was growing interest in these machines when more made their way into the second-hand market, and finally more and more documentation was released.

Since 2008/2009, work on the PA-RISC Linux port has become slower and quiet, similar to the other ports.

PA-RISC Linux/Puffingroup

The primary center of kernel and toolchain development is the offical PA-RISC Linux project. A range of resources is provided, including access to the source code, mailing lists for users and developers, installation instructions, an array of documentation and a hardware database.

Early work started in 1999 with the help of The Puffin Group, later employing several kernel and toolchain developers. Development was at first directed towards 32-bit systems; later on, with the help of Hewlett Packard, more modern machines were made available to developers, resulting in generally broader hardware and 64-bit support. Several important parts of the kernel PA-RISC support were written by HP employees participating in the project. The PA-RISC Linux affiliations changed throughout the last years, HP and developer support fluctuated but the port reached a stable state.

ESIEE

Contributed by Thibaut Varene

The PA-RISC Linux port effort started at ESIEE in December 1999, with Thierry Simonnet (who was then managing the General IT Resources Service at ESIEE) getting involved in the early stages of the port. By mid September 2000, Simonnet decided to get students involved, and he started a case study for students to participate in as part of their school curriculum. The study was conducted in parallel by HP Labs, who massively sponsored the effort of the school, being one of its long time key partner. This enabled the students to rapidly acquire skills and credibility, and the study was completed in February 2001, and presented at Linux Expo in Paris, and several months later at the Debian 1 Conference in Bordeaux, France. With its increasing success, the initial case study spawned into a larger project that was open to students either on their free time or as part of their classes, and more of them joined what was to be called the PATeam. From 2001 to the end of 2003, the team has been very active, doing numbers of development in the Linux kernel (writing drivers and improving overall stability).

Unfortunately, in 2004 and thereafter, ESIEE gradually reduced its support for the project, and nowadays it doesn't support it anymore, save for website and machines hosting.

4.3.5 References

Distributions

There were two popular Linux distributions that include the PA-RISC port throughout the 2000s: Debian and Gentoo.

- Debian included PA-RISC Linux from 2002 until 2012 as Debian/hppa in various releases from 3.0 to 4.0. Support for PA-RISC was dropped from Debian 6.0 on.
- Gentoo was the second distribution that included a PA-RISC port.

Documentation

- PA-RISC Linux: HARDWARE SUPPORT The PARISC-Linux Project (October 2019. Accessed March 2021)
- PA-RISC LINUX FAQ The PARISC-Linux Project (August 2018. Accessed March 2021)
- ESIEE PA/Linux Detailed Hardware Support ESIEE The PA/Linux Team (2016, archive.org mirror accessed February 2018)
- PA-RISC Linux hardware database The PARISC-Linux Project (June 2007. Accessed January 2009)
- PA-RISC Linux project page The PARISC-Linux Project (March 2021. Accessed March 2021)

Other documents

- Linux on PA-RISC. One Martini Too Many (.pdf) Matthew Wilcox (July 2000: Paper for OLS2000)

4.4 NetBSD/hppa

4.4.1 Overview

NetBSD is a free, open source Unix-like operating system with support for PA-RISC 1.1 32-bit computers in its NetBSD/hppa port since around 2005, called NetBSD/hp700 until the 7.0 release, as a "Tier II" port.

The port focuses on **32-bit** PA-RISC 1.1 computers and 64-bit PA-RISC 2.0 systems in 32-bit. The current effort is largely based on Michael Shalayeff's work on the OpenBSD/hppa kernel from 2004 to 2005 and updated OpenBSD code later on.

NetBSD/hppa is the least complete port of the three current open source systems, trailing both Linux and OpenBSD on PA-RISC.

4.4.2 Systems supported

NetBSD describes the following systems as supported (in the 7.0 release, as of 2015/2016), unsure if all are completely supported and tested.

Table 4.10: NetBSD/hppa supported systems

Class	Computers
700s	*705*, *710*, *712*, *715*, *720*, *730*, *750*, *725*, *735*, *755*
740s VME	*742*i, *743*i, *744*, *745*i, *745*, *747*i, *748*i, *748*
A-Class	A180, A180C
B-Class	B132L, B160L, B132L+, B180L+, B1000*, B2000*, B2600*
C-Class	C100, C110,C132L, C160L, C160*, C180*, C200*, C240*, C360*, C3000*, C3600*, C3700*
D-Class	D200, D210, D220, D230, D300, D310, D320, D330
E-Class	E25, E35, E45, E55 (apparently, and with serial console only, without SCSI)
J-Class	J200, J210, J280*, J282*, J2240*, J5000*, J5600*, J6000*, J6700*, J6750*, J7000*, J7600*
K-Class	K100, K200, K210, K220, K400, K410, K420
Portables	RDI PrecisionBook, SAIC Galaxy 1100

4.4.3 Hardware supported

Processors

32-bit PA-RISC 1.0 PA-7000, PA-7100, PA-7100LC, PA-7200 and PA-7300LC; some systems with 64-bit processors in 32-bit mode: PA-8000, PA-8200, PA-8500, PA-8600 and PA-8700.

Buses and chipsets

Most PCI, GSC and Runway buses and onboard bus controllers are supported.

Networking

On–board Ethernet and Fast-Ethernet network interfaces are supported; the FDDI sliders on the *735/755* are not supported. Expansion cards for the GSC/HSC and PCI bus slots with a supported Ethernet chipset (Intel i82596, DEC 21142/43 *Tulip*, Intel i8255x, Realtek 8120/8139, NE2000, SiS 900) could work.

Realtek RTL8150L USB-based Ethernet adapters are supported.

Storage

Storage I/O is supported via the NCR 53C700 narrow, NCR 53C710 Fast-Narrow or NCR 53C875 Ultra-Wide SE SCSI controllers. The on-board NCR 53C720 Fast-Wide HVD controllers are not supported.

GSC/HSC and PCI expansion cards with one of the 53C710 or 53C8xx (siop) SCSI chipsets, Adaptec 2940 (ahc) PCI and various Qlogic ISP PCI SCSI adapters should also work, however not necessarily for booting.

Graphics

SGC graphics (framebuffer). At the present there is no working X server.

Human I/O

Human I/O is supported via PS/2 and HIL.

Misc

Several PCI USB adapters from VIA and ALi have been tested and are known to work; they support USB mass-storage and Ethernet devices. The onboard Harmony audio system is supported.

4.4.4 References

Manuals

- INSTALL - Installation procedure for NetBSD/hppa for 7.0 release, NetBSD (September 2015: accessed January 2016)

Websites

- NetBSD/hppa official port page, NetBSD (October 2015, accessed January 2016)

Software

- NetBSD/hppa 7.0 (September 2015) ftp.netbsd.org

4.5 NeXTSTEP on PA-RISC

4.5.1 Overview

NeXTSTEP was a Unix operating system based on Mach microkernel with an advanced GUI developed in the 1980s and 90s. NeXTSTEP supported some PA-RISC computers in the 1994 in its 3.3 release in an effort to open up the operating system ecosystem to other hardware platforms.

Introduced in 1989 by NeXT, NeXTSTEP featured complete development and user environments, a unique GUI and special display system, the DPS Display Post Script. The underlying operating system core is a Mach microkernel, 4.3BSD compatible and runtime-extensible. In its early years, NeXTSTEP only ran on the so called "black hardware" , sophisticated and expensive custom NeXT designs, based on Motorola 68000. In 1991 "white hardware," Intel x86 PC technology was supported with Version 3.1. Development was continued and in 1994 Version 3.3 was released with support for RISC platforms including Sun SPARC and HP PA-RISC.

The support for PA-RISC was only brief and limited to a select set of workstations. NeXTSTEP itself, while revolutionary in aspects, did not have long-lasting commercial success. Parts of its ideas and technologies live on though in contemporary Mac OS.

4.5.2 Systems supported

NeXTSTEP runs on some of the 1990s 32-bit HP 9000/700 PA-RISC workstations with PA-7100 or PA-7100LC processors and ASP or LASI chipset.

- HP 9000 *712*, *715*, *725*, *735*, *755*

4.5.3 Hardware supported

NeXT supports most standard hardware of the supported workstations models:

- Diskspace requirements between 400 MB for a user environment to 700 MB for complete developer environment
- 32 MB to 64 MB RAM required, with a maximum of 256 MB supported
- All onboard graphics and CRX and CRX-24 supported
- HCRX and HCRX-24 graphics supported after installation of the NeXTSTEP 3.3 patches
- On *712* and *715/{64,80,100}* workstations only PS/2 keyboards supported, no HIL
- All other systems support HIL
- **Unsupported** on the *735/755* are the FWD (Fast/Wide Differential) SCSI subsystem and the optional FDDI network boards

4.5.4 References

Manuals

- NeXTstep 3.3 Network and System Administration Manual, NeXT Software Inc. (1994, mirrored at NeXTComputers.org. Accessed December 2019)
- NeXTstep 3.3 Developer Documentation Manuals, NeXT Software Inc. (1994, mirrored at NeXTComputers.org. Accessed December 2019)

Literature

- The NEXTSTEP/OpenStep FAQ, Bernhard Scholz (1996?, mirrored at levenez.com. Accessed December 2019)
- First NeXT RISCWorkstation: Our first look at NEXTSTEP on HP's low-cost pizza box, NeXTWORLD, April 1994

Software

There used to be a large software archive available at the Peanuts.org FTP server. It went offline about 2004-2005, without a known mirror. Other than that there is not much software available, other than contemporary open source of shareware software.

- NeXTSTEP Current Patch List (.pdf) Apple Computer, Inc (2006, mirrored at NeXTComputers.org. Accessed 8 January 2009)
- NeXTSTEP 3.3 "User" patch NS33RISCUserPatch3.tar (.tar) and its release notes NeXTSTEP 3.3 Patch 3 Overview (.pdf) Apple Computer, Inc (2006, mirrored at NeXTComputers.org. Accessed 8 January 2009)
- NeXTSTEP 3.3 "Developer" patch NS33DeveloperPatch2.tar (.tar)

4.6 OpenBSD/hppa

4.6.1 Overview

OpenBSD is an open source BSD Unix-like operating system ported to HP PA-RISC computers and focuses on 32-bit workstations and some 64-bit models running in 32-bit mode. Hardware support is solid for most on-board components and HP expansion options in support systems, in contrast to HP-UX there is significant support for generic/third-party devices.

The current OpenBSD/hppa version is 6.2, from October 2017.

Work on an OpenBSD port to PA-RISC HP 9000/700 systems was started by the late Michael Shalayeff around 1999. Main sources of information and code at that time were the previous porting efforts Lites/HPPA and MkLinux. The first more or less complete OpenBSD/hppa release was version 3.5, albeit still with limitations many unsupported machines and I/O devices.

NetBSD/hppa is heavily based on OpenBSD/hppa.

An OpenBSD/hppa64 port to support PA-RISC 2.0 computers running in 64-bit mode was started in 2007, but was discontinued after 2016.

Since 2008/2009, work on the OpenBSD/hppa port became rather quiet, similar to the other open-source PA-RISC ports.

4.6.2 Systems supported

Table 4.11: OpenBSD/hppa supported systems

Class	**Computers**
700s	*705*, *710*, *712*, *715*, *720*, *730*, *750*, *725*, *735*, *755*
740s VME	*742i*, *743i*, *744*, *745i*, *745*, *747i*, *748i*, *748*
A-Class	A180, A180C
B-Class	B132L, B160L, B132L+, B180L+, B1000*, B2000*, B2600*
C-Class	C100, C110,C132L, C160L, C160*, C180*, C200*, C240*, C360*, C3000*, C3600*, C3700*
D-Class	D220, D230, D320, D330
J-Class	J200, J210, J280*, J282*, J2240*, J5000*, J5600*, J6000*, J6700*, J6750*, J7000*, J7600*
K-Class	K100, K200, K210, K220, K400, K410, K420
Portables	RDI PrecisionBook, SAIC Galaxy 1100

Unsupported systems

Unsupported systems: PA-RISC 1.0 systems and the older HP 9000/800 servers like Nova, the E-Class, and the even older systems. Also in doubt are some of the newer 64-bit server systems with the **rp** designations, due to their chipsets and I/O systems.

4.6.3 Hardware supported

Processors

32-bit PA-RISC 1.0 PA-7000, PA-7100, PA-7100LC, PA-7200 and PA-7300LC; some systems with 64-bit processors in 32-bit mode: PA-8000, PA-8200, PA-8500, PA-8600 and PA-8700.

Buses and chipsets

All PCI, GSC and Runway buses and onboard bus controllers such as ASP, LASI, Dino/Cujo, U2/Uturn, Astro and Elroy on the above machines are supported. Additionally, Yenta-compatible PCI-Cardbus bridges are supported, as for instance found on the RDI Precisionbook.

Up to 2 GB of memory is supported.

ISA/EISA and HP-PB, VME buses and bus controllers are not supported.

Networking

All on-board Ethernet and Fast-Ethernet network interfaces on the above machines are supported; the FDDI on the 735/755 are not supported. Expansion cards for the GSC/HSC and PCI bus slots with a supported Ethernet chipset, like Intel i82596, DEC 21142/43 *Tulip*, Intel EtherExpress PRO/10 and PRO/100 series, Intel Gigabit chipsets, in various incarnations for the PCI bus, NE2000-compatible, 3Com 3c9xx EtherLink XL, should also work. PCMCIA and to a lesser extent Cardbus devices are supported in a compatible PCI-Cardbus bridges, including various WLAN and Ethernet cards. The OpenBSD port page has the current and complete list.

Storage

Storage is at the moment supported via either the NCR 53C700 Narrow, NCR 53C710 Fast-Narrow, NCR 53C720 Fast-Wide HVD/differential or the NCR 53C875 Ultra-Wide SE SCSI controllers. GSC/HSC and PCI expansion cards with one of the 53C7x0 or 53C8xx SCSI chipsets and Adaptec 2940 PCI SCSI adapters should also work, though are not neccessarily bootable.

Various newer PCI SCSI controllers based on Adaptec AHA and LSI Fusion-MPT chipsets are also supported, though also not bootable.

Graphics

All on-board graphics adapters are supported for text-mode via STI routines, similar to PC VGA BIOS, additionally the CRX, CRX-24, HCRX-8, HCRX-24, Visualize-EG and Visualize-FX (FX2, FX4 and FX6) graphics expansion boards on GSC and PCI are supported. X11 graphics capabilities are apparently working, in some way, since April 2015.

Human I/O and multimedia

Input/output is supported via PS/2 or HIL on-board interfaces, though not all HIL devices are supported.

Various USB devices are supported, including networking adapters and I/O devices attached to expansion USB controllers, PCMCIA/PCI.

The on-board 16-bit "Harmony" audio device, found on many PA-RISC workstations, is supported.

4.6.4 References

Websites

- OpenBSD/hppa official page, OpenBSD (October 2017: accessed February 2018)
- Discontinued OpenBSD/hppa64 official page, OpenBSD (2016. Accessed January 2020)

Software

There might be newer OpenBSD/hppa versions than listed below.

- OpenBSD/hppa 6.6 release (October 2019) ftp.openbsd.org
- OpenBSD/hppa snapshots ftp.openbsd.org
- Packages for add-on software see OpenBSD: Getting Packages
- Software is available through the OpenBSD Ports tree, a framework for open source software.

Manuals

- INSTALL.hppa (snapshot) installation instructions, OpenBSD (2020)
- INSTALL.hppa (6.6 release) installation instructions, OpenBSD (2019)

Other documents

- Michael Shalayeff: OpenBSD on PA-RISC talk NYCBUG (2007: NYCBUG 2005 talk. Accessed January 2009)

4.7 Research Operating Systems

With input from Mike Hibler (2008).

4.7.1 Overview

Several other operating systems have been ported to the PA-RISC platform over the time between the late 1980s and late 1990s. Most of them only reached development state and have long been unmaintained. Documentation is rare, some of it only in archives.

Table 4.12: PA-RISC R&D operating systems timeline

Year	HP	U Utah	OSF	Other
1988	HP Tut			
1989	HP Tut	HPBSD		
1990	HP OSF/1	HPBSD		Chorus (835)
1991	HP OSF/1	Mach 3/UX		Chorus (720)
1992				
1993		HPBSD 2.0		
1994		Mach 4/Lites	MK-PA 6.0	
1995			MK-PA 6.3	
1996		Mach 4/Lites II	MK-PA 7.x	
1997			MkLinux	

PA-RISC was used for many research projects in the late-1980s until the mid-1990s, a time when microkernels were a popular R&D target. Most alternative operating systems were thus Mach-based or leaned on it, with three major groups developing and researching operating systems:

- HP itself used PA-RISC early on for operating system research, known are the HP Tut and HP OSF/1 ports of Mach 2.0 to PA-RISC of the late-1980s.
- The University of Utah was a center of PA-RISC operating system research, with ports of Mach 3, Mach 4 and HPBSD.
- The OSF Open Group alliance ported its own OSF/1 Unix onto PA-RISC as MK-PA Mach research project, and used parts of that for the Mach-based MkLinux port.

Only MkLinux and Mach 4/Lites were publically available, the others required licenses for commercial or NDA source code they contained. Interest in Mach died down and these ports were all suceeded by open source systems in the early 2000s, that borrowed heavily from their code and documentation. Mach was commercialized eventually with NeXTSTEP, ported to PA-RISC in 1994, and iconic Mac OS X, itself based on Mach and influences from NeXTSTEP.

4.7.2 HP

HP Tut

Tut was an internal HP research project from around 1988-89 to port HP-UX onto a Mach microkernel. The project apparently never suceeded far and moved on to merging parts of Mach 2.0 under HP-UX 2.0 to get something close to resembling Mach on PA-RISC. HP Tut was the basis for various other porting efforts and PA-RISC research projects within and outside of HP.

HP OSF/1

Around 1990 an internal HP project ported an early 1.0 version of OSF/1 to PA-RISC. OSF/1 was the alternative Unix operating system by an alliance of DEC, IBM, HP and others to compete with AT&T's and Sun's System V Unix.

HP OSF/1 was developed by ex-Apollo staff, after Apollo was bought by HP, and ported an Mach 2.0 macrokernel to the early HP 9000/700 workstations, resulting in a fairly complete operating system, with proper hardware support and a usable desktop environment with Motif and other OSF/1 applications. The port was never distributed widely and sold commercially only for a short time before being withdrawn quickly. It was apparently used widely at the University of Utah.

4.7.3 University of Utah

HPBSD

HPBSD was developed between the late-1980s and mid-90s at the University of Utah by Mike Hibler and others, it grew out of a port of 4.3BSD to the 68k-based HP 9000/300 and 400 systems. HPBSD contains AT&T and HP source code and was never freely available. Organizations with the necessary license agreements with HP and AT&T were able to obtain bootable releases but distribution outside of the University of Utah was limited. HPBSD is an original 4.3BSD with additions from 4.4BSD and local modifications.

HPBSD supported the following hardware:

- *705*, *710*, *720*, *730*, *750* based on PA-*7000* processors
- *715*, *725*, *735*, *755* based on PA-*7100* processors
- *712*, *715*, *725*/100 based on PA-*7100LC* processors
- J200, J210[XC], C100, C110 based on PA-*7200* processors
- *Early HPBSD:*HP 9000/*835* server PA-RISC 1.0 NS-1 processor
- SCSI internal single-ended, internal fast-wide-differential, GSC based fast-wide-differential, and EISA fast-differential drives and DAT tapes, RS232 serial, builtin Ethernet, SGC FDDI board, GRX, CRX and Artist graphics, HIL and PS/2, audio

Taken from the original Utah webpage, and modified, with permission from Mike Hibler

HPBSD for 68k-based systems was born in 1987 when Mike Hibler started a port of 4.3BSD to the HP 9000/320 and 350 workstations at the University of Utah. Major development lasted until about 1991 with the final addition of Motorola 68040 support.

In the fall of 1989, Jeff Forys started work on a HP 9000/800 port based on the hybrid HP-UX/Mach kernel called Tut done as an experiment at HP Labs. By around February 1990 HPBSD was running on an 9000/835 and later that year was running solidly on the PA-RISC. For a short period of time in 1989-90, Mt Xinu also worked on the PA-RISC port and produced the first usable part of it, the boot loader, late in 1989. HPBSD used this boot loader. In 1990 another Mach project was spun off of HPBSD — the Mach 3/UX single server port for the 9000/835 sponsored by HP and primarily done by Bob Wheeler. Starting in May 1991, Leigh Stoller ported HPBSD to the HP 9000/720 workstation, after which support for PA-RISC 1.0 and the 9000/800 platform was dropped.

The last major development to HPBSD was the addition of the 4.4BSD kernel filesystem and networking code and the 4.4BSD ANSI-compliant C library. Jeff Forys started this in April 1992 and by early 1993 all of the University of Utah's HPBSD machines had been converted. This version was known as HPBSD 2.0. Since this merge included the NFS implementation done by Rick Macklem, all Sun encumbered code could be eliminated. In April 1993, a semi-formal release of HPBSD 2.0 was made to the 2-3 sites which had the necessary agreements with HP that were necessary to obtain the PA-RISC specific code. Since that time, active development of HPBSD had pretty much stopped. As of Summer 1999, there were less than ten HPBSD machines left: one 68k and the rest PA-RISC. The last significant efforts were to bring HP-UX compatibility up to 10.20 to run the JDK and to port a 3Com EISA 100 Mbit ethernet driver.

Mach 3

The Mach 3 port to PA-RISC called Mach 3/UX, from 1991 by Bob Wheeler of the University of Utah was one of the various Mach microkernel ports to PA-RISC. This port was supposed to accomplish what the previous, HP-internal HP Tut project aimed for — a proper port of Mach to PA-RISC. The sole target system was the HP 9000/835 server.

Ported were the Mach 3 microkernel with a proof-of-concept AT&T Unix System V kernel (personality) running as user-level server, with the Unix part originally done by CMU. The Mach 3/UX port never got very far, but code wound up later in Mach 4/Lites and probably MK-PA from OSF.

There might have been a separate University of Utah OSF/1 to PA-RISC porting effort (Mach 3/OSF/1), some sources suggest a short-lived project to port Mach 3.0 and OSF/1 1.0.4 to PA-RISC.

Mach 4

The University of Utah Flux Research Group ported the original Mach microkernel with a 4.4BSD-Lites server around 1994 to the PA-RISC architecture, based on the work of the Mach 3/UX project, and called it Mach 4/Lites. There was not much support provided and few enhancements made over the years, and it was quickly discontinued in favor of other projects both at Utah University and elsewhere, for example the MkLinux port. The project was seen from the beginning not as a complete operating system but rather as a snapshot for developers.

Mach 4/Lites supported the following hardware:

- 705, 710, 720, 730, 750 based on PA-7000 processors
- 715, 725, 735, 755 based on PA-7100 processors
- 712 apparently with serious issues, 715 based on PA-7100LC processors
- Internal single-ended and fast-wide different SCSI drives and tapes, RS232 serial, builtin Ethernet, GRX and CRX graphicss, Artist on 712/715 probably, HIL and PS/2 keyboard/mouse
- Unsupported: FDDI networking, EISA expansion cards and devices, parallel ports, audio, tele-share port on 712, floppy drives and all other hardware

Taken from the original Utah webpage, and modified, with permission from Mike Hibler

Mach 4/Lites supported the PA-RISC 1.1 HP 9000/700 platform with freely distributable source, binaries, and boot image for a complete Mach kernel that includes some of Utah's then-recent (though not exploited) research, the Lites BSD-based single-server, `include` directories and libraries, and a complete GNU toolchain for the ELF object format. In addition, there are several other PA-RISC-related

device drivers, kernel components and utilities and a fairly complete 4.4BSD-lite user environment. The entire system was self-built on Mach 4/Lites.

The operating system kernel is based on a Mach kernel, derived from CMU's (Carnegie Mellon University) MK83 release, and is loosely referred to as Mach 4. It contains some initial work done at Utah as part of the ARPA-funded *Fast and Flexible Mach Systems* work. In particular it contains a prototype implementation of migrating threads and a basic framework for signature-based remote procedure calls, a fundamental component of the presentation/interface work. None of these features is used either by the Lites server or within the kernel itself.

The PA-RISC-specific part includes all the necessary interrupt, exception, and locore system call handling code, a pmap module, and device drivers for the VSC and GSC bus based workstations. The only kernel or server component provided only as a binary library and not in source form is the floating point emulation code which handles operations and exceptional conditions not done in hardware. The `libmach` and `libcthreads` libraries are also included with the necessary changes for PA-RISC support.

Also included is additional code never integrated into Mach 4, that was part of Utah's earlier Mach 3/UX and HPBSD ports or HP OSF/1. The former includes bus configuration and rudimentary device drivers for the CIO bus based workstations and servers as well as a remote kernel/task debugging facility developed by Convex. The latter includes some basic EISA support and alternative LAN drivers.

The Unix which runs on top of the Mach kernel is Lites, an 4.4BSD-lite Berkeley Unix operating system personality provided by the Lites server/emulator. Lites is a user-mode, single-task implementation of BSD Unix which runs on top of a Mach micro-kernel, developed at Helsinki University of Technology HUT in Finland.

4.7.4 OSF

MK-PA

OSF/1 was the third "flavor" of Unix besides System V and BSD, developed by a consortium between DEC, IBM and HP. The OSF Open Group Research Institute ported OSF/1 to PA-RISC in the mid-1990s as a research project, focusing on 32-bit HP 9000/700 workstations and servers. Research releases were MK6.0-PA in 1994, MK6.3-PA in July 1995 and MK7-PA and MK7.2-PA in 1996. Porting was supported by HP in some way. MK-PA was never distributed or released widely, but used for research purposes a lot, including for ARPA projects (to include radar tracking). Obtaining MK-PA from OSF RIrequired an OSF/1 source license.

Hardware support focused on PA-RISC 1.1 700s workstations, support for the 800s PA-RISC 1.0 servers was dropped from the original Mach 3/UX code base. MK-PA as research project had as its main objectives to demonstrate: PA-RISC as OSF RI reference platform, performance parity between HP-UX and MK based systems, HP-UX binary compatibility, high-speed networking capability. Performance was similar between HP-UX and MK-PA at that time. HP-UX compatibility was provided for HP-UX 9.05 on the MK-PA 7.1 release; compatibility for HP-UX 10 was apparently achieved with MK-PA 7.2. OSF MK 7.2 ran on both Intel x86 and HP PA-RISC and featured OSF/1 1.3.1 commands and libraries.

The version of Mach 3 used by the OSF porting effort contained several of the Mach 4 enhancements of the University of Utah and probably used parts of the Mach 3/UX PA-RISC codebase. Parts of the MK-PA port were used as the base of the OSF port of Linux onto OSF Mach, MkLinux.

MK-PA supported the following hardware;

- 710, 720, 730 based on PA-7000 processors

- 715, 725, 735, 755 based on PA-7100 processors
- 712, 715, 725/100 based on PA-7100LC processors
- J200, J210[XC], based on PA-7200 processors
- Additionally Interphase FDDI board, EISA Ethernet boards, HP Labs GSC bus Myrinet board
- MK 7.2: Myrinet networking, FDDI, DIPC and CORDS

MkLinux

MkLinux was a research project from the mid-1990s by the Open Group/OSF to port a Linux kernel as server onto a Mach microkernel, the Open Group pmk1.1. The project built on the previous MK-PA Mach 3 port. Other parts were integrated from the PA-RISC kernel sources from the Utah University, including Mach 3/UX and Mach 4/Lites. The port improved the underlying OSF PA-RISC/Mach kernel from MK-PA and put a Linux 2.0 kernel as server personality on top, replacing BSD/Lites from the previous efforts. Included were X11R6 patches, the GNU ELF compiler and debugger and complete `/usr` and `/var` directories.

MkLinux was the first free operating system that truly ran on PA-RISC hardware, in contrast to the various Mach ports, which suffered from unfinished development and a lot of bugs on PA-RISC. However, the system was rather slow, did not support shared libraries, software support was rather rudimentary and at the time of its active development PA-RISC workstations were not largely available to private end-users.

MkLinux supported the following hardware and systems.

- 705, 710, 720, 730, 750 based on PA-7000 processors
- 715 (no /33), 725, 735, 755 based on PA-7100 processors
- 712, 715, 725/100 based on PA-7100LC processors
- C100, C110 based on PA-7200 processors
- SCSI internal single-ended, internal fast-wide-differential, GSC-based fast-wide-differential, and EISA fast-differential, RS232 serial, builtin Ethernet, GRX, CRX and Artist graphics, HIL and PS/2, audio

4.7.5 Other

Chorus

Chorus was a micro-kernel operating system by INRIA, started in 1979. A development effort was made to port it to PA-RISC in 1990-1991 at the Oregon Graduate Institute OGI.

The porting effort, a funded research project by Jonathan Walpole, was based on the Chorus v3.3 nucleus kernel with the Chorus/MiX v3.2 on it for the HP 9000/834 system. Hardware support was rather limited, with apparently no network interfaces or disk devices supported and console I/O depending on PDC and IODC routines. Code from various earlier projects was used, including from HP-UX 2.0 and HP Tut, HP-UX on 2.0 Mach. The port succeeded up to the stage that Unix shells and various system calls worked, but no access to file systems was possible.

A later porting project was started by Jon Inouye, also from Oregon Graduate Institute, to port the Chorus/MiX v3.2 with the newer v3.4 nucleus to the PA-RISC 1.1 9000/720 workstation a popular target for OS/Unix porting efforts at that time. The port did not progress very far, as it supported few device drivers. In contrast to the earlier HP 9000/834 port it used HP-UX 8.0 as a base.

Both ports were never distributed as they contained various copyrighted/licensed source code from HP, Chorus, USL, and others.

4.7.6 References

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4.8 PA-RISC Operating Systems History

The history of PA-RISC operating systems started in parallel to the design and development of PA-RISC and HP 9000 computers. Many Unix and research operating systems were made available in the late-1980s, first the early commercial HP-UX PA-RISC releases, followed by a plethora of research and development projects centered around the Mach microkernel and BSD Unix versions.

4.8.1 Commercial

HP-UX: The story of HP-UX Unix started before PA-RISC, with versions for the early HP 9000 lineup — the HP FOCUS systems. From the late 1980s on, HP-UX was available on the first PA-RISC server computers (800s), with HP-UX 7.0 released in 1989. Updated and enhanced version soon followed, with the BSD-influenced HP-UX 8.0 and 9.0 from the early 1990s supporting most early HP 9000 700s and 800s.

The new HP-UX 10 was released a few years later, followed in quick sucession by 10.20 and 10.30. Due to feared Y2K issues in earlier versions the, popular HP-UX 10.20 was made available free of charge for HP 9000 owners for a while. The modernized HP-UX 11 was released from the mid-1990s on, with a "true 64-bit kernel" that still supported many 32-bit PA-RISC systems and hardware. The focus of HP-UX shifted soon to the newer "lettered" (A-Class, B-Class, ...) and rp/rx 64-bit and Itanium servers in the 11i HP-UX versions during the early 2000s. HP-UX 11i v2 integrated PA-RISC and Itanium into a single operating system stream while HP-UX was relegated more and more to specialized server roles.

NeXTSTEP: NeXTSTEP on PA-RISC was a commercial Mach-based operating system from the 1990s with an Unix userland and an extremely modern GUI, ported by NeXT Inc. to PA-RISC in 1994. Support for some 32-bit PA-RISC machines was available in Version 3.3, which was designed for the HP 9000 712 workstation. Both NeXTSTEP and its support for PA-RISC were wound down soon thereafter — with parts of NeXTSTEP ending up in the 2000s reincarnation of Mac OS.

Other operating systems: There were a few other notable operating systems that ran on PA-RISC. HP's own MPE business mainframe operating system was ported from the HP 3000 CISC platform to PA-RISC with MPE/XL and MPE/iX, with several releases from 1988 to 2002. Another PA-RISC operating system by HP was HP-RT, a real-time operating system geared towards the HP 9000 740 series VME board workstations.

Several third-party operating systems for PA-RISC were developed by several companies for their own line of computers. This includes Convex SPP/UX, a heavily modified Mach-based operating system, which looks familiar to HP-UX but is a completely different design, for the Convex/HP Exemplar SPP1000, 1200 and 1600 line of mainframes. The fault-tolerant Continuum servers from Stratus were shipped with either Stratus FTX, a System V Unix, or Stratos VOS, a transaction-processing oriented system.

Development: There were apparently development efforts in the mid-1990s to port Microsoft Windows NT to PA-RISC. Several magazine articles ("HP edges towards NT support" in Computerworld 12/13/93) and USEnet posts around 1993 mentioned as much that HP was pursuing a PA-RISC port to NT and even conducted a "back-room" presention of a PA-7100LC workstation running Windows NT. Around the same time, a two-year effort to port the NetWare operating system to PA-RISC was mentioned.

Apparently there was a prototype port of HP-UX to x86 hardware, at a time when the future of HP-UX and the sole surving hardware platform Itanium came in doubt during the early 2010s — PA-RISC was long gone then.

4.8.2 Open source

Linux: A native Linux port to PA-RISC was started in 1998 and gained momentum when HP started helping with equipment and documentation in 1999. The main Linux port quickly superseded the earlier Mach-based MkLinux. Because of HP's assistance, the machines targeted at that time were newer than what other ports supported, like the A180, B180 and 64-bit PA 2.0 systems.

PA-RISC support was included in the mainstream kernel, and shipped with Debian and Gentoo distributions as official ports. During the 2010s however, support declined and development was scaled back, resulting in the eventual removal of PA-RISC from official distributions. PA-RISC Linux still has the broadest support for systems and hardware from the current open source efforts.

BSD: Work on an OpenBSD port to PA-RISC on HP 9000/700 systems was started by Michael Shalayeff around 1999. His porting efforts were based a lot on source code and information from the previous PA-RISC research projects Lites/HPPA and MkLinux. The first complete OpenBSD/hppa release was version 3.5, with PA-RISC having been supported since on most 32-bit workstation, some 64-bit workstations and some servers. An OpenBSD/hppa64 port to support PA-RISC 2.0 computers running natively in 64-bit mode was started in 2007, but never took off.

NetBSD/hppa is a free, open source Unix-like operating system, and supports PA-RISC computers since around 2005, called NetBSD/hp700 until the 7.0 release, as a "Tier II" port. The port focuses on 32-bit PA-RISC 1.1 computers and 64-bit PA-RISC 2.0 systems in 32-bit. The current effort is largely based on Michael Shalayeff's work on the OpenBSD/hppa kernel from 2004 to 2005 and updated OpenBSD code later on.

4.8.3 Research

R&D: As soon as PA-RISC was released in the late 1980s, academic and industrial research projects started operating systems ports to PA-RISC. The premier among them was HPBSD from the University of Utah which was a port of 4.3BSD and later 4.4BSD to early 800s servers and specially the early 700s workstations. HPBSD contained commercial AT&T and HP code, and was never freely available.

Several ports of the **Mach** microkernel were undertaken during the early 1990s, with HP Tut using Mach 2.0 and the University of Utah trying Mach 3 and Mach 4. Porting efforts for OSF/1, the alliance Unix operating system from DEC, IBM, HP and others to compete with AT&T and Sun's System V Unix, started around 1990. HP itself ported OSF/1 to PA-RISC, which was never widely available commercially. This port was superseded in the mid-1990s by the OSF RI Open Group Research Institute with several releases of MK-PA. All of the Mach ports were never really used widely as production systems, but formed the basis for other research projects and later the BSD and Linux ports.

Early Linux support on PA-RISC built upon the MkLinux research project from the mid-1990s by the Open Group/OSF, that ported a Linux kernel onto a Mach microkernel, which in turn built on the previous MK-PA OSF/1 port to PA-RISC.

4.8.4 Timeline

The approximate timeline of operating system development is as follows.

Table 4.13: PA-RISC operating systems timeline

Year	HP-UX	Linux	OSD	NSD	HP-BSD	Mach3	Mach4	OSF/1	MkLinux	NeXT
1988	✧				✧					
1989	■■				■					
1990	✧				■			✧		
1991	■				✧	✧		✧		
1992	■				✧					
1993	✧				■					
1994	✧						✧	■		■
1995	■						✧	■		
1996	■■						■	■		
1997	■■								✧	
1998	✧	✧							✧	
1999	✧	✧	✧							
2000	■■	✧	✧							
2001	■	✧	✧							
2002	■	■	✧							
2003	✧	✧	■							
2004	✧	✧	■■	✧						
2005	■	■■	■■	■						
2006	✧	✧	■■	■						
2007	■	■■	■■	■						
2008	✧	■	■■							
2009	✧	■	■■	■						
2010	✧		■■	■						
2011	✧	✧	■■							
2012	✧	✧	■■	■■						
2013	✧	✧	■■	■						
2014	✧	✧	■■							
2015	✧	✧	■■	■						
2016	✧	✧	■■							
2017	✧	✧	■■	■						
2018	✧	✧	■■	■■						
2019	✧	✧	■■	■						

4.8.5 Further reading

- ◈ More information on the PA-RISC Operating Systems page.
- ◈ Release timelines and dates on the PA-RISC Timeline page.
- ◈ HP started then spiked HP-UX on x86 project, The Register, May 2012

Chapter 5

Appendix

5.1 Print History

Table 5.1: OpenPA print releases changes

Release	Files changed	Lines added	removed	modified
2.8	92	1336	1113	1456
2.7	48	96	360	1244
2.6	90	210	1753	9378
2.5	91	2048	1.936	7636
2.4	70	818	1.668	2422
2.3	52	1141	269	1306
2.2	69	1.080	917	1975
2.1	18	315	29	170
2.0	56	2262	183	2377
1.2	-	-	-	-
1.1	14	157	406	775
1.0	-	-	-	-

Changes in Second Edition 2.7 since the last edition (2018):

- HP 9000 and PA-RISC Computers Story article added
- OpenPA.net turned twenty in 2019
- Many updates to PA-RISC computers articles
- HP 9000 520 FOCUS article updated
- HP 9000 743/744 VME article update and extended for VXI boards
- PA-RISC in US Navy DTC and TAC information added
- Many revisions and corrections (thanks!)
- HP Agilent 16600 and 16700 PA-RISC logic analyzers article added

Changes in Second Edition 2.6 since the last edition (2016):

- HP 9000 and PA-RISC history article
- Operating system reference table
- Major housecleaning of almost all articles
- Separate PA-RISC chipsets pages
- Extended chipset and system architecture information

Changes in Second Edition 2.5 since Second Edition 2.4:

- (2.5.1) BSD operating system support updated (OpenBSD and NetBSD)
- PA-RISC System Architecture section integrated into the Chipset section, with multiple PA-RISC platforum designs from the early 1980s to mid-2000s
- PA-RISC hardware and operating systems timeline added

- ◈ PA-RISC entry dates and prices added
- ◈ Many dead links to official documentation and resources removed (404)
- ◈ Wording and spelling corrections, several sections rewritten
- ◈ Stats: 91 files changed, 2048 insertions, 1936 deletions 7636 modifications (lines)

Changes in Second Edition 2.4 since Second Edition 2.3:

- ◈ Architecture and ISA pages improved
- ◈ HP-UX 11.x sections extended
- ◈ Processor sections improved
- ◈ Buses and SCSI sections improved
- ◈ Chipset section extended (Stretch, zx1, others)
- ◈ T-Class pages added
- ◈ Corrections to the PA-RISC OEM systems
- ◈ Operating systems pages updated
- ◈ Wording and spelling corrections

Changes in Second Edition 2.3 since Second Edition 2.2:

- ◈ Wax I/O adapter added
- ◈ CPU bus attachments of the PA-RISC processors added
- ◈ Memory and I/O controllers updated and extended
- ◈ HP-UX and other operating system support updated and revised
- ◈ Many pages rewritten and updated with general corrections
- ◈ More price and introduction date information for various HP 9000 systems

Changes in Second Edition 2.2 since Second Edition 2.1:

- ◈ Removal of several outdated pages: PDC Boot-ROM (only relevant to older systems, incomplete), LED error codes (same), Expansion cards (outdated and incomplete, just a collection of HP part numbers) and Memory modules (same)
- ◈ Almost all other pages have been updated and/or rewritten, especially the hardware sections (processors, chipsets, buses)

Changes in Second Edition 2.1 (October 2008) since Second Edition 2.0 (22 pages added):

- ◈ Convex Exemplar SPP1000, SPP1200 and SPP1600 (XA and CD) mainframes added
- ◈ HP/Convex Exemplar SPP2000 (S-Class/X-Class) mainframes added
- ◈ 3rd party PA-RISC computers information added: more Hitachi (3050RX, 3500 and 9000V OEM) and Mitsubishi (MELCOM ME RISC) and Oki (OKITAC 9000) OEM systems (relabeled HP)

- HP 9000/V2200 and V2250 Exemplar mainframes added
- HP 9000/V2500 and V2600 Exemplar mainframes added
- Cover page and several post-release spelling corrections

Changes in Second Edition 2.0 (May/June 2008) since First Edition 1.2 (about 90 pages added and almost all other updated/modified):

- HP Itanium/IA64 servers added: rx1600/rx1620, rx2600/rx2620, rx4610, rx4640 and rx5670
- HP Itanium/IA64 workstations added: i2000, zx2000 and zx6000
- Much improved Other PA-RISC Operating Systems page (Mach 4/Lites, HPBSD, OSF/1, Mach 3, Chorus, and others)
- HP 9000 N4000 (rp7400) server section added
- Stretch and Cell-based (Superdome) chipset sections added
- HP 9000 N4000 (rp7405 and rp7410) server section added
- HP 9000 L1500 (rp5430) and L3000 (rp5470) server section added
- HP 9000 rp3410 and rp3440 (*rp3400 series*) server section added
- HP 9000 rp4410 and rp4440 (*rp4400 series*) server section added
- Reworked and more detailed HP 9000/500 FOCUS systems section
- Expanded and corrected early PA-RISC history/servers section
- Early PA-RISC 1.0 processors (TS-1, NS-1, NS-2, CMOS26B/PCX) section added
- Much improved and expanded Stratus Continuum servers section
- Winbond W89K and W90K embedded PA-RISC processors section added
- Synchronize with online OpenPA.net content
- Typographic polishing (TEX and in the HTML sources)
- Improvements to and streamlining of the HTML-to-PDF conversion process
- Removal of (book-format) DIN A5 print format

Changes in Release 1.2 (December 2007) since First Edition 1.1:

- Typographic modifications for limited print edition

Changes in Release 1.1 (November 2007) since First (Prerelease) Edition 1.0:

- Text formatting and positioning
- Typographic improvements
- Addition of a (book-format) DIN A5 print format
- PA-RISC History page added, covering the early PA-RISC days
- Catch-up with all changes/updates from the OpenPA online edition (about one year worth of updates)

First (Prerelease) Edition 1.0 was published in July 2006.

5.2 PA-RISC Benchmarks

Assorted benchmark results, compiled with available **SPEC benchmark** results for PA-RISC and Itanium systems. Multi-processor configurations are noted (2P, 4P etc.), otherwise the results are from single-processor systems.

Results from three different benchmark sets: **SPEC92**, **SPEC95** and **SPEC2000**.

Table 5.2: PA-RISC computers assorted SPEC benchmarks results

Model	**SPEC92 int/fp**	**SPEC95 int/fp**	**SPEC95** *rate* **int/fp**	**SPEC2000 int/fp**	**SPEC2000** *rate* **int/fp**
705	21.9/33.0				
710	31.6/47.6	1.0/1.4			
712/60	67.0/85.3	2.1/2.7	18.7/23.9		
712/80	97.1/123.3	3.1/3.5	28.1/32.0		
712/100	117.2/144.2	3.8/4.1	33.8/36.3		
715/33	32.5/52.4	1.0/1.6			
715/50	49.2/78.8	1.5/2.5			
715/64	80.6/109.4	2.5/3.3			
715/75	82.6/127.2	2.5/3.8			
715/80	96.3/123.2	3.0/3.5			
715/100	115.1/138.7	3.8/4.0	30.0/38.3		
715/100XC	132.2/184.6	4.5/4.7	40.9/42.3		
720	36.4/58.2	1.2/2.0	14.1/18.2		
725/50		1.5/2.5			
725/75		2.5/3.8			
725/100		3.8/4.0			
730	47.8/75.4	1.5/2.3			
735/99		3.2/4.1	29.4/35.8		
735/125		4.0/4.6	36.3/40.9		
742i/50		1.5/2.5			
743i/64		2.5/3.3			
743i/100		3.8/4.0			
744/132L		6.4/6.7			
744/165L		7.9/7.6			
745i/50		1.5/2.5			
745i/100		3.2/4.1			
745/132L		6.4/6.7			
745/165L		7.9/7.6			
747i/50		1.5/2.5			
747i/100		3.2/4.1			
748i/64		2.5/3.3			
748i/100		3.8/4.0			
748/132L		6.4/6.7			
748/165L		7.9/7.6			
750	48.1/75.0	1.5/2.3			
755/99		3.2/4.0	29.4/35.8		
755/125		4.0/4.6	36.3/40.9		
A180					
A180C		9.2/8.6			

A500-5X (rp2450)				422/414	2P: 9.3/7.6
A500-7X (rp2470)				581/	6.74/ 2P: 12.9/
B132L		6.4/6.7	58.1/60.3		
B132L+		6.8/7.2	61.5/64.6		
B160L		7.7/7.6	69.7/68.1		
B180L+		9.2/9.4	83.0/84.8		
B1000		23.9/39.3	217/378		
B2000		31.8/52.4	286/472	332/357	3.8/4.1
B2600				403/440	4.7/5.1
C100		5.0/6.6	44.8/59.4		
C110		6.0/8.1	54.0/73.3		
C132L		6.4/6.7	58.1/60.3		
C160L		7.7/7.6	69.7/68.1		
C160		10.4/16.3	93.6/147		
C180		11.8/18.7	107/169		
C200		14.2/21.4	129/193		
C240		17.1/25.4	156/229		
C360		26.0/28.1	234/252		
C3000		31.8/52.4	287/471	313/321	
C3600		42.0/64.0	379/576	432/433	5.0/5.0
C3650				508/542	5.9/6.3
C3700				604/576	7.0/6.7
C3750				678/674	
C8000				1001?/	
D200	115/146	2.2/2.9	19.2/25.8		
D210	152/194	3.7/4.1	33.6/36.7		
D220		6.6/6.7	59.2/60.5		
D230		7.9/7.6	70.8/68.3		
D250	144/218	5.0/6.8	45.1/61.0 2P: 89.0/106		
D260			2P: 114/143		
D270		10.4/15.0	93.9/135 2P: 184/190		
D280		12.3/17.4	111/157 2P: 219/221		
D300	115/146	2.2/2.9	19.2/25.8		
D310	152/194	3.7/4.1	33.6/36.7		
D320		6.6/6.7	59.2/60.5		
D330		7.9/7.6	70.8/68.3		
D350	144/218	5.0/6.8	45.1/61.0 2P: 89.0/106		
D360			2P: 114/143		
D370		10.4/15.0	93.9/135 2P: 184/190		
D380		12.3/17.4	111/157 2P: 219/221		
D390		15.5/25.5			
E25	45.0/66.7				
E35	65.6/98.5				

E45	82.1/122.9				
E55	108.0/163.4				
F10	22.0/36.6				
F20	33.6/56.1				
F30 G30 H30 I30	37.8/62.4				
G40 H40 I40	65.2/91.3				
G50 H50 I50	100.0/158.5				
G60 H60 I60	108.8/195.3				
G70 H70 I70	108.8/195.3				
Galaxy 1100 80 MHz (SAIC)		3.1/3.5			
i2000 733 MHz 2 MB				/623	/7.2
i2000 733 MHz 4 MB					/577
i2000 800 MHz 2 MB				/655 2P:/658	/7.6 2P: /13.2
i2000 800 MHz 4 MB				365/610	
J200		5.0/4.5	44.8/61.3 2P: 64.5/105		
J210		6.0/5.4	54.0/73.4 2P: 77.5/126		
J210XC		6.4/5.7	57.6/81.5 2P: 82.8/142		
J280		11.8/19.3	107/174		
J282					
J2240		17.4/26.3	157/237 2P: 307/349		
J5000		32.5/54.0	302/486 2P: 579/744		
J5600		42.6/62.7	384/564 2P: 758/847		
J6000		42.6/62.7	384/564 2P: 758/847	441/433	2P: 9.7/8.0
J6700		57.6/85.9		603/581	2P: 13.4/10.5
J6750				676/651	2P: 14.9/11.5
J7000		32.5/54.0	302/486 2P: 579/744		
K100		4.9/6.8			
K200		4.9/6.8	44.3/61.2 2P: 87.9/117 4P: 174/198		

K210		5.9/8.1	53.3/73.4 2P: 106/140 4P: 210/238		
K220		6.4/9.1	57.7/82.0 2P: 114/157 4P: 228/275		
K250		10.7/18.8	96.0/169 2P: 189/279 4P: 375/383		
K260		11.8/20.2	107/182 2P: 212/297 4P: 418/398		
K370		14.6/23.0	132/207 2P: 261/322 4P: 519/434 6P: 767/489		
K380		17.4/28.5	157/257 2P: 312/398 4P: 610/532 6P: 902/604		
K400		4.9/6.8	44.3/61.2 2P: 87.9/117 4P: 174/198		
K410		5.9/8.1	53.3/73.4 2P: 106/140 4P: 210/238		
K420		6.4/9.1	57.7/82.0 2P: 114/157 4P: 228/275		
K450		10.7/18.8	96.0/169 2P: 189/279 4P: 375/383		
K460		11.8/20.2	107/182 2P: 212/297 4P: 418/398		
K570		14.6/23.0	132/207 2P: 261/322 4P: 519/434 6P: 767/489		
K580		17.4/28.5	157/257 2P: 321/398 4P: 610/532 6P: 902/604		
L2000-44 *(rp5450)*		33.7/72.3			
L3000-5X rp2470				388/376	4.5/4.4 2P: 8.9/8.3 4P: 17.4/14.5
L3000-7X rp2470				581/	6.7/ 2P: 12.9/
N4000-6X rp7400				493/489	5.7/5.7 2P: 11.3/10.4 4P: 22.1/19.3 8P: 42.6/30.5

N4000-7X rp7400				551/524	6.4/6.1 2P: 12.5/11.0 4P: 24.6/20.5 8P: 46.7/32.1
PrecisionBook 132 (RDI)		6.5/6.5			
PrecisionBook 160 (RDI)		7.8/7.4			
PrecisionBook 180 (RDI)		9.2/9.4			
R380		12.3/17.4			
R390		15.5/25.5			
rp3440 1 GHz dualcore					1P/2C: 18.7/19.2 2P/4C: 37.1/32.6
rp4440 1 GHz dualcore					1P/2C: 18.6/19.3 2P/4C: 37.0/34.7 4P/8C: 73.2/55.4
rx1600 1.0 GHz 1.5 MB				837/1382	9.71/16.0 2P: 19.1/27.6
rx1620-2 1.3 GHz 3.0 MB				1178/2214	13.7/25.7 2P: 27.0/42.7
rx1620-2 1.6 GHz 3.0 MB				1452/2692	16.8/31.2 2P: 33.2/50.4
rx2600 900 MHz 1.5 MB				674/1151	7.8/ 2P: 15.5/
rx2600 1.0 GHz 3.0 MB				810/1427	9.4/ 2P: 18.7/
rx2600 1.3 GHz 3.0 MB				1073/1808	12.4/ 2P: 24.8/
rx2600 1.5 GHz 6.0 MB				1408/2119	15.3/ 2P: 30.5/
rx2620-2 1.3Hz 3.0 MB				1170/2229	13.6/15.9 2P: 26.9/27.7
rx2620-2 1.6Hz 3.0 MB				1408/2553	16.3/29.6 2P: 32.3/48.5
rx2620-2 1.6Hz 6.0 MB				1535/2675	17.8/31.0 2P: 35.5/51.5
rx4610 800 MHz 4 MB				379/701	4.4/8.1 2P: /14.2 4P: /22.4
rx4640 1.3 GHz 3.0 MB				1132/1891	13.1/21.9 2P: 25.8/37.9 4P: 51.4/57.4
rx4640 1.5 GHz 6.0 MB				1404/2161	16.3/25.1 2P: 32.5/43.2 4P: 64.2/65.6
rx4640-8 1.5 GHz 4.0? MB				1372/2502	15.9/29 2P: 31.7/48.3 4P: 62.2/70.5
rx4640-8 1.6 GHz 9 MB				1590/2712	4P: 72.5/77.9

rx5670 900 MHz 1.5 MB				673/1151	7.81/13.3 2P: 15.5/24.5 4P: 30.4/38.7
rx5670 1.0 GHz 3.0 MB				807/1431	9.36/16.6 2P: 18.6/30.7 4P: 36.8/49.3
rx5670 1.3 GHz 3.0 MB				1066/1814	12.4/21.0 2P: 24.5/37.3 4P: 48.6/57.2
rx5670 1.5 GHz 6.0 MB				1312/2108	1P: 15.2/24.5 2P: 30.3/42.6 4P: 60.0/66.4
T520		5.2/	1P: 47.2/ 2P: 93.8/ 4P: 186/ 8P: 363 12P: 531		
T600		11.8/14.9	1P: 106/134 2P: 211/263 4P: 418/510 6P: 617/735 8P: 814/915 10P: 1003/1043 12P: 1192/1151		
V2200		13.8/22.1	1P: 125/ 4P: 484/755 8P: 964/1380 12P: 1442/1909 16P: 1865/2312		
V2250		16.4/24.8	16P: 2209/2471		
V2500			16P: 4002 32P: 7481		
V2600			16P: 5164 32P: 9315		
SPP1000/XA (Convex)		3.3/4.0			
SPP1200/XA (Convex)	/185				
SPP1600/CD (Convex)			8P: 290/383 16P: 541/744 32P: 996/1444		

SPP2000 (Convex) S-Class X-Class		11.8/18.7	92.5/141 2P: 183/276 4P: 363/524 6P: 539/739 8P: 713/935 10P: 867/1085 12P: 1012/1220 16P: 1307/1413		
zx2000 900 MHz				668/1086	/12.6
zx6000 900 MHz				669/1139	7.8/13.2 2P: 15.4/23.9
zx6000 1.0 GHz				807/1422	/16.5 2P: /30
zx6000 1.5 GHz				1315/2106	15.2/24.4 2P: 30.4/42.4